NOIV1SN5000A

VITA 5000 5.3 Megapixel 75 FPS Global Shutter CMOS Image Sensor

ON Semiconductor®

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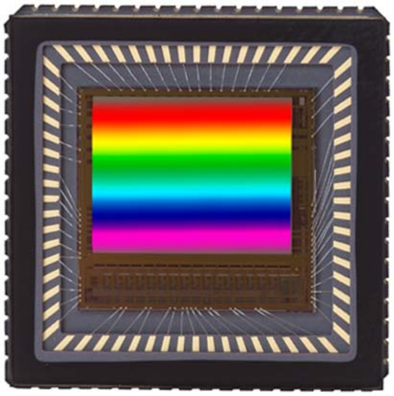


Figure 1. VITA 5000 Photo

Features

- QSXGA: 2592 x 2048 Active Pixels
- 4.8 μm x 4.8 μm Pixel Size
- 1 inch Optical Format
- Monochrome (SN) or Color (SE)
- 75 Frames per Second (fps) at Full Resolution (LVDS)
- On-chip 10-bit Analog-to-Digital Converter (ADC)
- 8-bit or 10-bit Output Mode
- Eight LVDS Serial Outputs
- Random Programmable Region of Interest (ROI) Readout
- Pipelined and Triggered Global Shutter, Rolling Shutter
- On-chip Fixed Pattern Noise (FPN) Correction
- Serial Peripheral Interface (SPI)
- Automatic Exposure Control (AEC)
- Phase Locked Loop (PLL)
- High Dynamic Range (HDR)
- Dual Power Supply (3.3 V and 1.8 V)
- 0°C to 70°C Operational Temperature Range
- 68-pin LCC
- 1000 mW Power Dissipation in 10-bit Mode
- These Devices are Pb−Free and are RoHS Compliant

Applications

- Machine Vision
- Motion Monitoring
- Security
- Barcode Scanning (2D)

Description

The VITA 5000 is a 1 inch Quad Super eXtended Graphics Array (QSXGA) CMOS image sensor with a pixel array of 2592 by 2048.

The high sensitivity 4.8 μm x 4.8 μm pixels support pipelined and triggered global shutter readout modes and can also be operated in a low noise rolling shutter mode. In rolling shutter mode, the sensor supports correlated double sampling readout, reducing noise and increasing the dynamic range.

The sensor has on-chip programmable gain amplifiers and 10-bit A/D converters. The integration time and gain parameters can be reconfigured without any visible image artifact. Optionally the on-chip automatic exposure control loop (AEC) controls these parameters dynamically. The image's black level is either calibrated automatically or can be adjusted by adding a user programmable offset.

A high level of programmability using a four wire serial peripheral interface enables the user to read out specific regions of interest. Up to 8 regions can be programmed, achieving even higher frame rates.

The image data interface consists of eight LVDS lanes, facilitating frame rates up to 75 frames per second. Each channel runs at 620 Mbps. A separate synchronization channel containing payload information is provided to facilitate the image reconstruction at the receiver end.

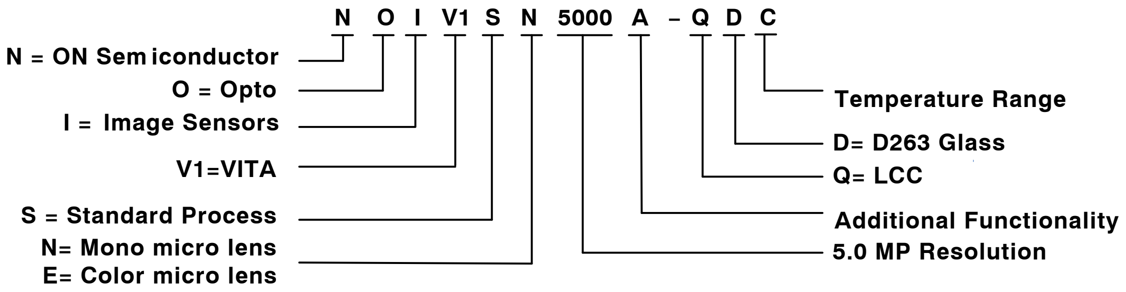
The VITA 5000 is packaged in a 68-pin LCC package and is available in a monochrome and color version.

Contact your local ON Semiconductor office for more information.

ORDERING INFORMATION

Part Number	Mono/Color	Package
NOIV1SN5000A-QDC	Mono micro−lens	68−pin LCC
NOIV1SE5000A-QDC	Color micro−lens	

ORDERING CODE DEFINITION



PACKAGE MARK

Following is the mark on the bottom side of the package with Pin 1 to the left center

Line 1: **NOIV1xx 5000A** where xx denotes mono micro lens (SN) or color micro lens (SE) option

Line 2: **-QDC**

Line 3: **AWLYYWW**; where line 3 is the lot traceability as indicated below

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SPECIFICATIONS

Key Specifications

Table 1. GENERAL SPECIFICATIONS

Parameter	Specification
Pixel type	Global shutter pixel architecture
Shutter type	Pipelined and triggered global shutter, rolling shutter
Frame rate at full resolution	75 fps
Master clock	62 MHz when PLL is used, 310 MHz (10-bit) / 248 MHz (8-bit) when PLL is not used
Windowing	8 Randomly programmable windows. Normal, sub-sampled and binned read-out modes
ADC resolution [1]	10-bit, 8-bit
LVDS outputs	8 data + sync + clock
Data rate	8 x 620 Mbps (10-bit) / 8 x 496 Mbps (8-bit)
Power dissipation	1000 mW in 10-bit mode
Package type	68-pin LCC

Table 2. ELECTRO−OPTICAL SPECIFICATIONS

Parameter	Specification
Active pixels	2592 (H) x 2048 (V)
Pixel size	4.8 μm x 4.8 μm
Optical format	1 inch
Conversion gain	0.072 LSB10/e^- 85 μV/e^-
Dark noise	2.2 LSB10, 30e^- in global shutter 0.9 LSB10, 14e^- in rolling shutter
Responsivity at 550 nm	24 LSB10 /nJ/cm^2, 4.6 V/lux.s
Parasitic Light Sensitivity (PLS)	<1/450
Full well charge	13700 e^-
Quantum efficiency	53% at 550 nm
Pixel FPN	rolling shutter: 1.0 LSB10 global shutter: 2.0 LSB10
PRNU	< 2% of signal
MTF	60% @ 630 nm - X-dir & Y-dir
PSNL @ 25°C	100 LSB10/s, 1360 e^-/s
Dark signal @ 25°C	4.5 e^-/s, 0.33 LSB10/s
Dynamic range	60 dB in rolling shutter mode 53 dB in global shutter mode
Signal to Noise Ratio (SNR max)	41 dB

Table 3. RECOMMENDED OPERATING RATINGS (Note 2)

Symbol	Description	Min	Max	Units
T_J	Operating temperature range	0	70	°C

Table 4. ABSOLUTE MAXIMUM RATINGS (Notes 3 and 4)

Symbol	Parameter	Min	Max	Units
ABS (1.8 V supply group)	ABS rating for 1.8 V supply group	–0.5	2.2	V
ABS (3.3 V supply group)	ABS rating for 3.3 V supply group	–0.5	4.3	V
T_S	ABS storage temperature range	0	150	°C
	ABS storage humidity range at 85°C		85	%RH
Electrostatic discharge (ESD)	Human Body Model (HBM): JS−001−2010	2000		V
	Charged Device Model (CDM): JESD22−C101	500		
LU	Latch-up: JESD−78	140		mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. The ADC is 11−bit, down−scaled to 10−bit. The VITA 5000 uses a larger word−length internally to provide 10−bit on the output.
2. Operating ratings are conditions in which operation of the device is intended to be functional.
3. ON Semiconductor recommends that customers become familiar with, and follow the procedures in JEDEC Standard JESD625−A. Refer to Application Note AN52561. Long term exposure toward the maximum storage temperature will accelerate color filter degradation.
4. Caution needs to be taken to avoid dried stains on the underside of the glass due to condensation. The glass lid glue is permeable and can absorb moisture if the sensor is placed in a high % RH environment.

Table 5. ELECTRICAL SPECIFICATIONS

Boldface limits apply for $T_J = T_{MIN}$ to T_{MAX}, all other limits T_J = +30°C. (Notes 5, 6 and 7)

Parameter	Description	Min	Typ	Max	Units
Power Supply Parameters					
vdd_33	Supply voltage, 3.3 V	**3.0**	3.3	**3.6**	V
Idd_33	Current consumption 3.3 V supply		235		mA
vdd_18	Supply voltage, 1.8 V	**1.6**	1.8	**2.0**	V
Idd_18	Current consumption 1.8 V supply		115		mA
vdd_pix	Supply voltage, pixel	**3.0**	3.3	**3.6**	V
Ptot	Total power consumption at vdd_33 = 3.3 V, vdd_18 = 1.8 V		1000		mW
Pstby_lp	Power consumption in low power standby mode. (See Silicon Errata on page 67)			50	mW
Popt	Power consumption at lower pixel rates	Configurable			
I/O - LVDS (EIA/TIA-644): Conforming to standard/additional specifications and deviations listed					
fserdata	Data rate on data channels DDR signaling - 4 data channels, 1 synchronization channel;			620	Mbps
fserclock	Clock rate of output clock Clock output for mesochronous signaling			310	MHz
Vicm	LVDS input common mode level	0.3	1.25	2.2	V
Tccsk	Channel to channel skew (Training pattern allows per channel skew correction)			50	ps
Electrical/Interface					
fin	Input clock rate when PLL used			62	MHz
fin	Input clock when LVDS input used			310	MHz
tidc	Input clock duty cycle when PLL used	40	50	60	%
tj	Input clock jitter		20		ps
fspi	SPI clock rate when PLL used at fin = 62 MHz			10	MHz
Frame Specifications - Global Shutter					
fps	Frame rate at full resolution (global shutter)			75	fps
fps_roi1	Xres x Yres = 2592 x 1944			80	fps
fps_roi2	Xres x Yres = 2048 x 2048			92	fps
fps_roi3	Xres x Yres = 1024 x 1024			310	fps
fps_roi4	Xres x Yres = 640 x 480			860	fps
fps_roi5	Xres x Yres = 512 x 512			910	fps
fps_roi6	Xres x Yres = 256 x 256			2260	fps
FOT	Frame Overhead Time		45		µs
ROT	Row Overhead Time		1.1		µs
fpix	Pixel rate (8 channels at 62 Mpix/s)			496	Mpix/s

5. All parameters are characterized for DC conditions after thermal equilibrium is established.
6. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is recommended that normal precautions be taken to avoid application of any voltages higher than the maximum rated voltages to this high impedance circuit.
7. Minimum and maximum limits are guaranteed through test and design.

For recommendations on power supply management guidelines, refer to application note AN65464: VITA 5000 HSMC Cyclone Reference Board Design Recommendations.

Color Filter Array

The VITA color micro−lens sensors (SE) are processed with a Bayer RGB color pattern as shown in Figure 2. Pixel (0,0) has a red filter situated to the bottom left.

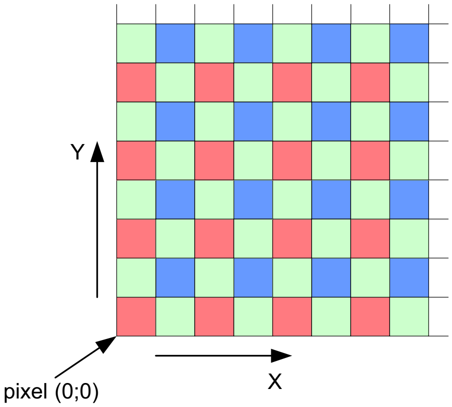


Figure 2. Color Filter Array for the Pixel Array

Spectral Response Curve

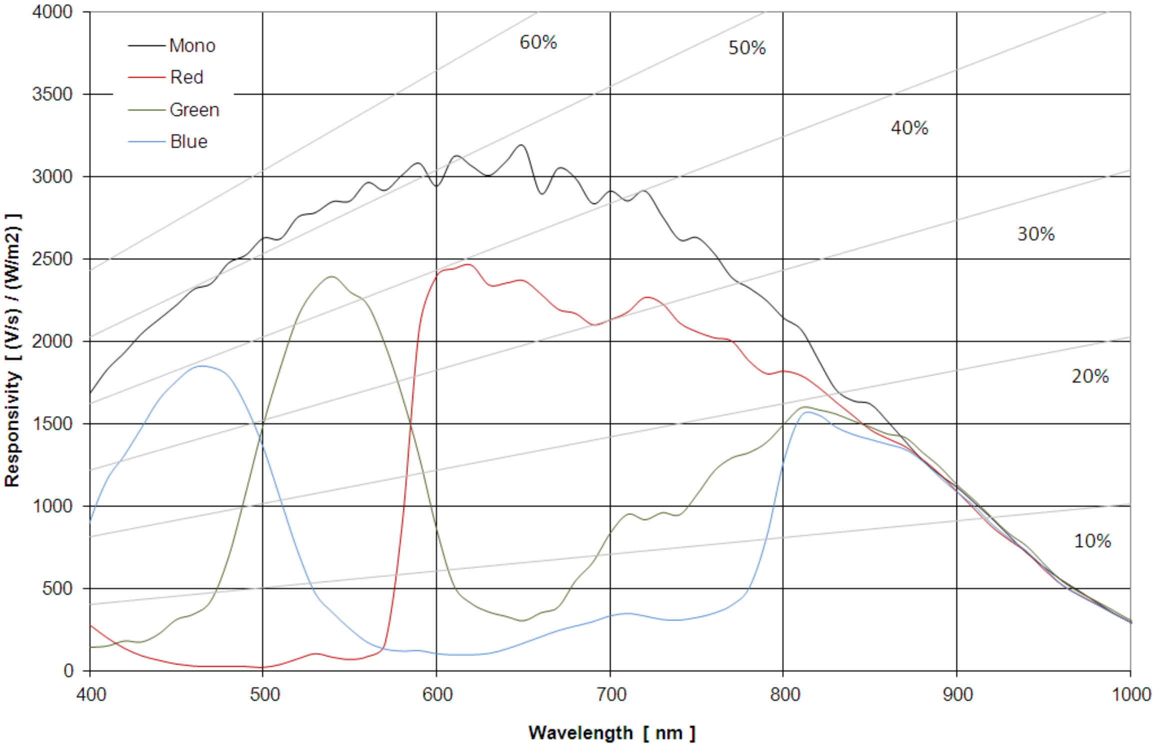


Figure 3. Spectral Response Curve

Note that green pixels on a Green−Red (Green 1) and Green−Blue (Green 2) row have similar responsivity to wavelength trend as is depicted by the legend “Green”.

OVERVIEW

Figure 4 gives an overview of the major functional blocks of the sensor respectively. The system clock is received by the CMOS clock input. A PLL generates the intenal, high speed, clocks, which are distributed to the other blocks. Optionally, the sensor can also accept a high speed LVDS clock, in which case the PLL will be disabled.

The sequencer defines the sensor timing and controls the image core. The sequencer is started either autonomously (master mode) or on assertion of an external trigger (slave mode). The image core contains all pixels and readout circuits. The column structure selects pixels for readout and performs correlated double sampling (CDS) or double sampling (DS). The data comes out sequentially and is fed into the analog front end (AFE) block. The programmable gain amplifier (PGA) of the AFE adds the offset and gain. The output is a fully differential analog signal that goes to the ADC, where the analog signal is converted to a 10-bit data stream. Depending on the operating mode, eight or ten bits are fed into the data formatting block. This block adds synchronization information to the data stream based on the frame timing. The data then goes to the low voltage serial (LVDS) interface block which sends the data out through the I/O ring.

On-chip programmability is achieved through the Serial Peripheral Interface (SPI). See the Register Map on page 44 for register details.

A bias block generates bias currents and voltages for all analog blocks on the chip. By controlling the bias current, the speed-versus-power of each block can be tuned. All biasing programmability is contained in the bias block.

The sensor can automatically control exposure and gain by enabling the automatic exposure control block (AEC). This block regulates the integration time along with the analog and digital gains to reach the desired intensity.

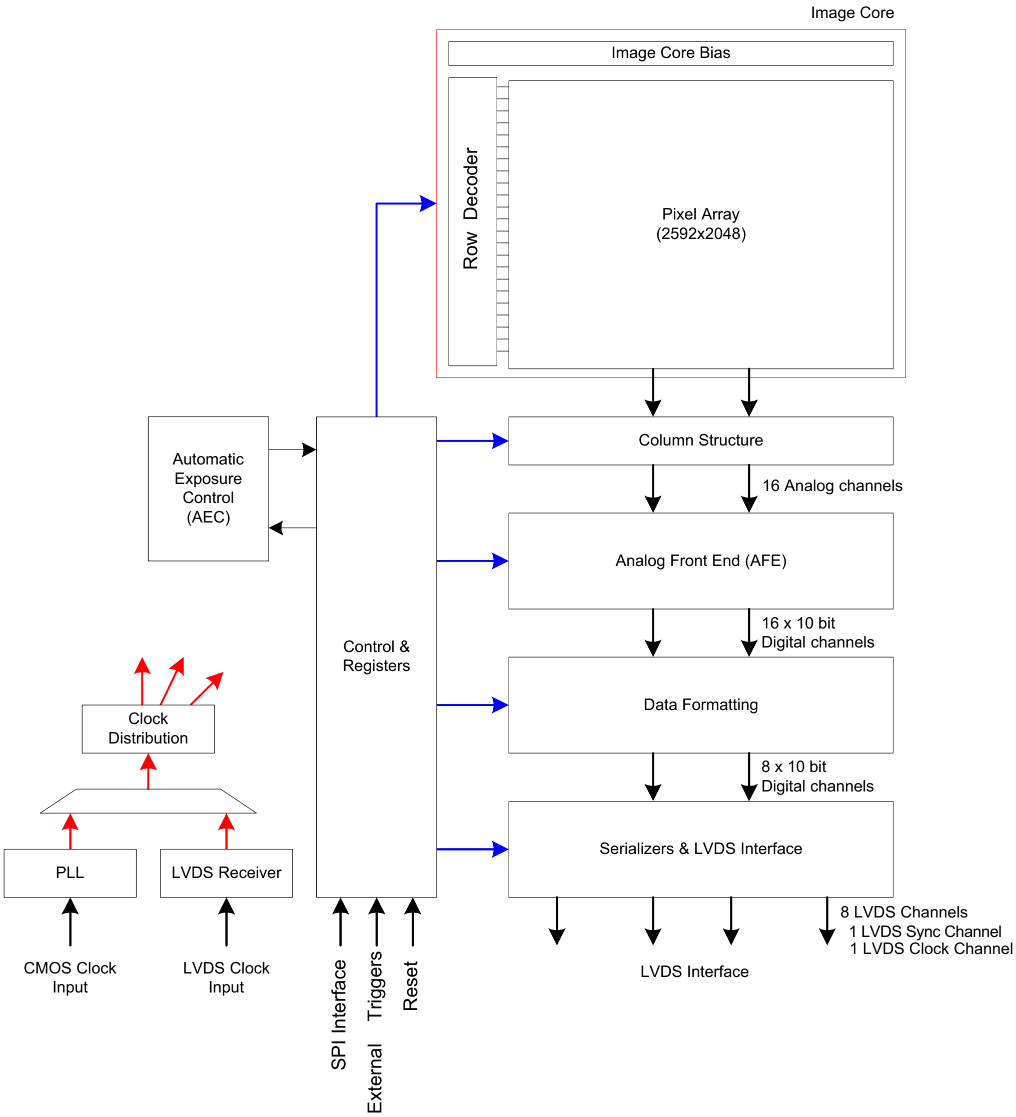


Figure 4. Block Diagram

Image Core

The image core consists of:

- Pixel Array
- Address Decoders and Row Drivers
- Pixel Biasing

The pixel array contains 2592 (H) x 2048 (V) readable pixels with a pixel pitch of 4.8 μm. Four dummy pixel rows and columns are placed at every side of the pixel array to eliminate possible edge effects. The sensor uses a 5T pixel architecture, which makes it possible to read out the pixel array in global shutter mode with double sampling (DS), or in rolling shutter mode with correlated double sampling (CDS).

The function of the row drivers is to access the image array line by line, or all lines together, to reset or read the pixel data. The row drivers are controlled by the on-chip sequencer and can access the pixel array in global and rolling shutter modes.

The pixel biasing block guarantees that the data on a pixel is transferred properly to the column multiplexer when the row drivers select a pixel line for readout.

Phase Locked Loop

The PLL accepts a (low speed) clock and generates the required high speed clock. Optionally this PLL can be bypassed. Typical input clock frequency is 62 MHz.

LVDS Clock Receiver

The LVDS clock receiver receives an LVDS clock signal and distributes the required clocks to the sensor.

Typical input clock frequency is 310 MHz in 10-bit mode and 248 MHz in 8-bit mode. The clock input needs to be terminated with a 100 Ω resistor.

Column Multiplexer

All pixels of one image row are stored in the column sample-and-hold (S/H) stages. These stages store both the reset and integrated signal levels.

The data stored in the column S/H stages is read out through 8 parallel differential outputs operating at a frequency of 31 MHz.

At this stage, the reset signal and integrated signal values are transferred into an FPN-corrected differential signal.

The column multiplexer also supports read-1-skip-1 and read-2-skip-2 mode. Enabling this mode can speed up the frame rate, with a decrease in resolution.

Bias Generator

The bias generator generates all required reference voltages and bias currents that the on-chip blocks use. An external resistor of 47 kΩ, connected between pin IBIAS_MASTER and gnd_33, is required for the bias generator to operate properly.

Analog Front End

The AFE contains 8 channels, each containing a PGA and a 10-bit ADC.

For each of the 8 channels, a pipelined 10-bit ADC is used to convert the analog image data into a digital signal, which is delivered to the data formatting block. A black calibration loop is implemented to ensure that the black level is mapped to match the correct ADC input level.

Data Formatting

The data block receives data from two ADCs and multiplexes this data to one data stream. A cyclic redundancy check (CRC) code is calculated on the passing data.

A frame synchronization data block transmits synchronization codes such as frame start, line start, frame end, and line end indications.

The data block calculates a CRC once per line for every channel. This CRC code can be used for error detection at the receiving end.

Serializer and LVDS Interface

The serializer and LVDS interface block receives the formatted (10-bit or 8-bit) data from the data formatting block. This data is serialized and transmitted by the LVDS output driver.

In 10-bit mode, the maximum output data rate is 620 Mbps per channel. In 8-bit mode, the maximum output data rate is 496 Mbps per channel.

In addition to the LVDS data outputs, two extra LVDS outputs are available. One of these outputs carries the output clock, which is skew aligned to the output data channels. The second LVDS output contains frame format synchronization codes to serve system-level image reconstruction.

Sequencer

The sequencer:

- Controls the image core. Starts and stops integration in rolling and global shutter modes and control pixel readout.
- Operates the sensor in master or slave mode.
- Applies the window settings. Organizes readouts so that only the configured windows are read.
- Controls the column multiplexer and analog core. Applies gain settings and subsampling modes at the correct time, without corrupting image data.
- Starts up the sensor correctly when leaving standby mode.

Automatic Exposure Control

The AEC block implements a control system to modulate the exposure of an image. Both integration time and gains are controlled by this block to target a predefined illumination level.

OPERATING MODES

The VITA 5000 sensor is able to operate in the following shutter modes:

- Global Shutter Mode
  - ♦ Pipelined Global Shutter
    - Master
    - Slave
  - ♦ Triggered Global Shutter
    - Master
    - Slave
- Rolling Shutter Mode

Global Shutter Mode

In the global shutter mode, light integration takes place on all pixels in parallel, although subsequent readout is sequential. Figure 5 shows the integration and readout sequence for the synchronous shutter. All pixels are light sensitive at the same period of time. The whole pixel core is reset simultaneously and after the integration time all pixel values are sampled together on the storage node inside each pixel. The pixel core is read out line by line after integration. Note that the integration and readout can occur in parallel or sequentially.

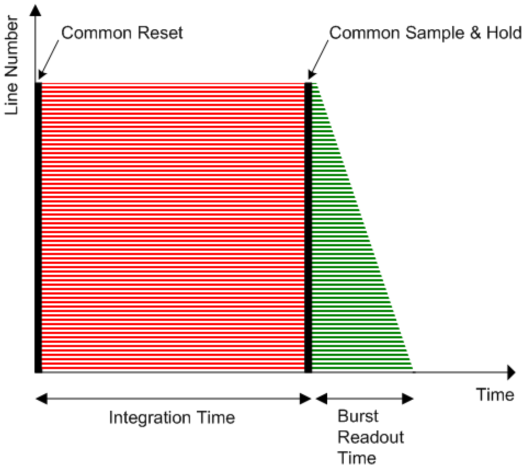


Figure 5. Global Shutter Operation

Pipelined Global Shutter

In pipelined global shutter mode, the integration and readout are done in parallel. Images are continuously read and integration of frame N is ongoing during readout of the previous frame N-1. The readout of every frame starts with a Frame Overhead Time (FOT), during which the analog value on the pixel diode is transferred to the pixel memory element. After the FOT, the sensor is read out line per line and the readout of each line is preceded by the Row Overhead Time (ROT). Figure 6 shows the exposure and readout time line in pipelined global shutter mode.

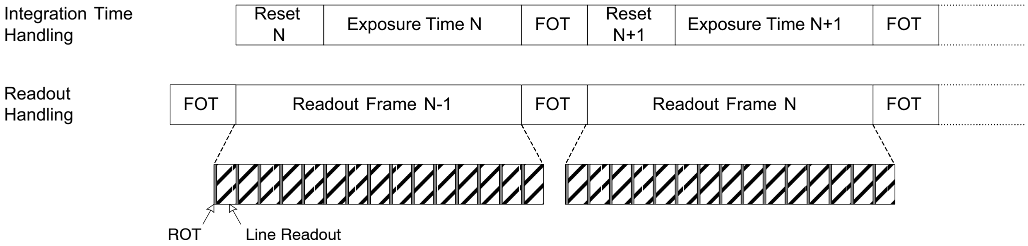


Figure 6. Integration and Readout for Pipelined Shutter

- Master

In this operation mode, the integration time is set through the register interface and the sensor integrates and reads out the images autonomously. The sensor acquires images without any user interaction.

- Slave

The slave mode adds more manual control to the sensor. The exposure time registers are ignored in this mode and the integration time is controlled by an external pin. As soon as the control pin is asserted, the pixel array goes out of reset and integration starts. The integration continues until the external pin is de-asserted by the system. Now, the image is sampled and the readout is started. Figure 7 shows the relation between the external trigger signal and the exposure/readout timing.

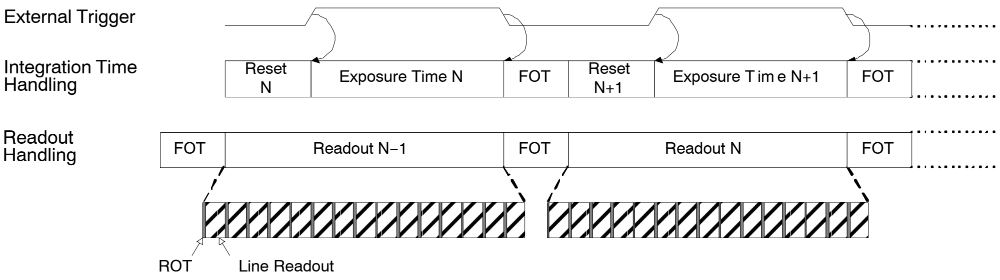


Figure 7. Pipelined Shutter Operated in Slave Mode

Triggered Global Shutter

In this mode, manual intervention is required to control both the integration time and the start of readout. After the integration time, indicated by a user controlled pin, the image core is read out. After this sequence, the sensor goes to an idle mode until a new user action is detected.

The three main differences with the pipelined global shutter mode are

- Upon user action, one single image is read.
- Integration and readout are done sequentially. However, the user can control the sensor in such a way that two consecutive batches are overlapping, that is, having concurrent integration and readout.
- Integration and readout is under user control through an external pin.

This mode requires manual intervention for every frame. The pixel array is kept in reset state until requested.

The triggered global mode is also controlled in a master or slave mode fashion.

- Master

In this mode, a rising edge on the synchronization pin is used to trigger the start of integration and readout. The integration time is defined by a register setting. The sensor autonomously integrates during this predefined time, after which the FOT starts and the image array is readout sequentially. A falling edge on the synchronization pin does not have any impact on the readout or integration and subsequent frames are started again for each rising edge. Figure 8 shows the relation between the external trigger signal and the exposure/readout timing.

If a rising edge is applied on the external trigger before the exposure time and FOT of the previous frame is complete, it is ignored by the sensor.

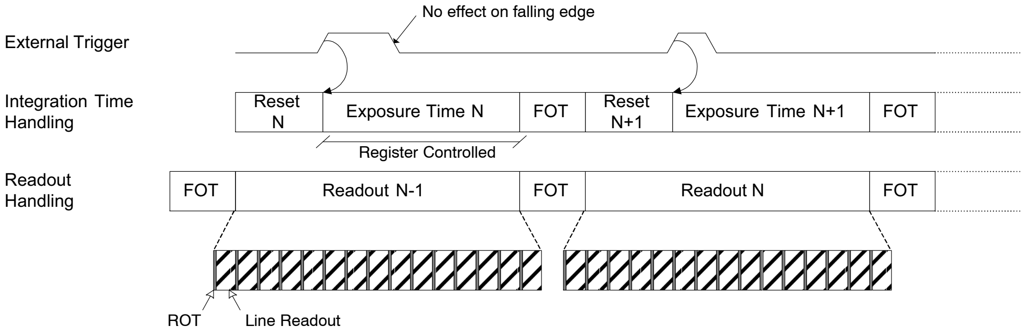


Figure 8. Triggered Shutter Operated in Master Mode

- Slave

Integration time control is identical to the pipelined shutter slave mode. An external synchronization pin controls the start of integration. When it is de-asserted, the FOT starts. The analog value on the pixel diode is transferred to the pixel memory element and the image readout can start. A request for a new frame is started when the synchronization pin is asserted again.

Rolling Shutter Mode

Another shutter mode supported by the sensor is the rolling shutter mode. The shutter mechanism is an electronic rolling shutter and the sensor operates in a streaming mode similar to a video. This mechanism is controlled by the on-chip sequencer logic. There are two Y pointers. One points to the row that is to be reset for rolling shutter operation, the other points to the row to be read out. Functionally, a row is reset first and selected for read out sometime later. The time elapsed between these two operations is the exposure time.

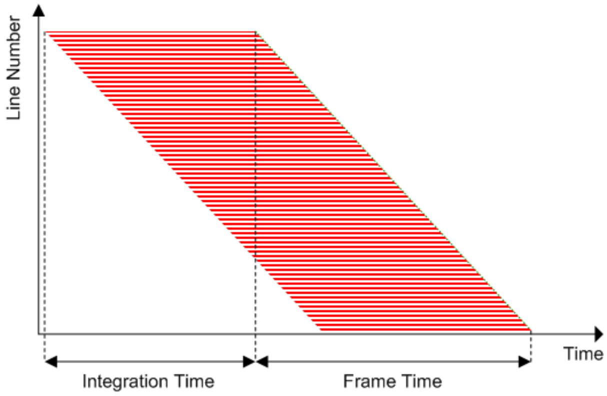


Figure 9. Rolling Shutter Operation

Figure 9 schematically indicates the relative shift of the integration times of different lines during the rolling shutter operation. Each row is read and reset in a sequential way. Each row in a particular frame is integrated for the same time, but all lines in a frame 'see' a different stare time. As a consequence, fast horizontal moving objects in the field of view give rise to motion artifacts in the image; this is an unavoidable property of a rolling shutter.

In rolling shutter mode, the pixel Fixed Pattern Noise (FPN) is corrected on-chip by using the CDS technique. After light integration on all pixels in a row is complete, the storage node in the pixel is reset. Afterwards the integrated signal is transferred to that pixel storage node. The difference between the reset level and integrated signal is the FPN corrected signal. The advantage of this technique, compared to the DS technique used in the global shutter modes, is that the reset noise of the pixel storage node is cancelled. This results in a lower temporal noise level.

SENSOR OPERATION

Flowchart

Figure 10 shows the sensor operation flowchart. The sensor can be in six different ‘states’. Every state is indicated with the oval circle. These states are:

- Power off
- Low power standby
- Standby (1)
- Standby (2)
- Idle
- Running

These states are ordered by power dissipation. In ‘power-off’ state, the power dissipation is minimal; in ‘running’ state the power dissipation is maximal.

On the other hand, the lower the power consumption, the more actions (and time) are required to put the sensor in ‘running’ state and grab images.

This flowchart allows the trade-off between power saving and enabling time of the sensor.

Next to the six ‘states’ a set of ‘user actions’, indicated by arrows, are included in the flowchart. These user actions make it possible to move from one state to another.

Sensor States

Power Off

In this state, the sensor is inactive. All power supplies are down and the power dissipation is zero.

Low Power Standby

In low power standby state, all power supplies are on, but internally every block is disabled. No internal clock is running (PLL / LVDS clock receiver is disabled).

All register settings are unchanged.

Only a subset of the SPI registers is active for read/write in order to be able to configure clock settings and leave the low power standby state. The only SPI registers that should be touched are the ones required for the ‘Enable Clock Management’ action described in Enable Clock Management – Part 1 on page 14

Standby (1)

In standby state, the PLL/LVDS clock receiver is running, but the derived logic clock signal is not enabled.

Standby (2)

In standby state, the derived logic clock signal is running. All SPI registers are active, meaning that all SPI registers can be accessed for read or write operations. All other blocks are disabled.

Idle

In the idle state, all internal blocks are enabled, except the sequencer block. The sensor is ready to start grabbing images as soon as the sequencer block is enabled.

Running

In running state, the sensor is enabled and grabbing images. The sensor can be operated in different rolling/global master/slave modes.

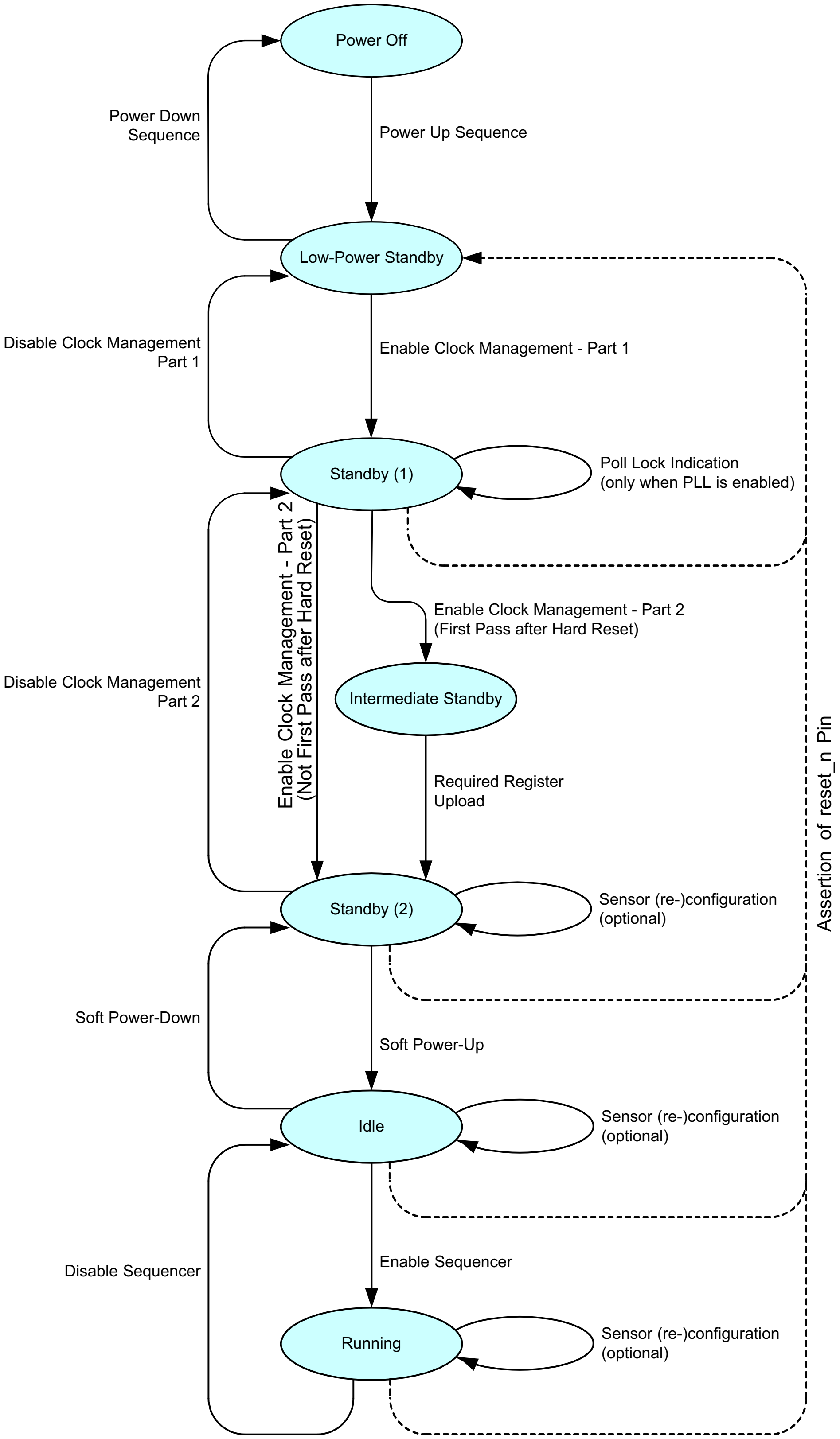


Figure 10. Sensor Operation Flowchart

User Actions: Power Up Functional Mode Sequences

Power Up Sequence

Figure 11 shows the power up sequence of the sensor. The figure indicates that the first supply to ramp-up is the vdd_18 supply, followed by vdd_33 and vdd_pix respectively. It is important to comply with the described sequence. Any other supply ramping sequence may lead to high current peaks and, as consequence, a failure of the sensor power up.

The clock input should start running when all supplies are stabilized. When the clock frequency is stable, the reset_n signal can be de-asserted. After a wait period of 10 μs, the power up sequence is finished and the first SPI upload can be initiated.

NOTE: The ‘clock input’ can be the CMOS PLL clock input (clk_pll), or the LVDS clock input (lvds_clock_inn/p) in case the PLL is bypassed.

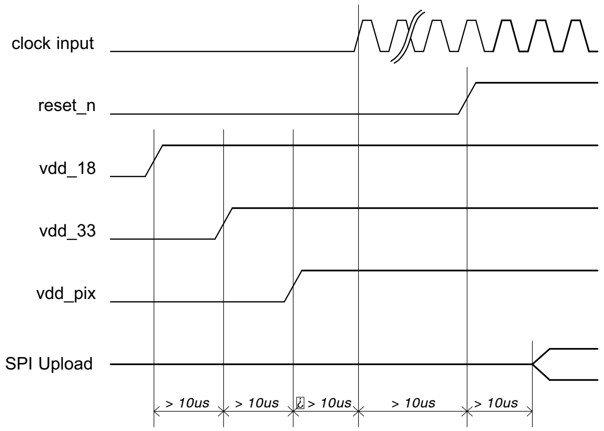


Figure 11. Power Up Sequence

Enable Clock Management − Part 1

The ‘Enable Clock Management’ action configures the clock management blocks and activates the clock generation and distribution circuits in a pre-defined way. First, a set of clock settings must be uploaded through the SPI register. These settings are dependent on the desired operation mode of the sensor.

Table 6 shows the SPI uploads to be executed to configure the sensor for 8-bit serial and 10-bit serial mode, with and without the PLL.

In the serial modes, if the PLL is not used, the LVDS clock input must be running.

It is important to follow the upload sequence listed in Table 6.

Use of Phase Locked Loop

If PLL is used, the PLL is started after the upload of the SPI registers. The PLL requires (dependent on the settings) some time to generate a stable output clock. A lock detect circuit detects if the clock is stable. When complete, this is flagged in a status register.

Check this flag by reading the SPI register. When the flag is set, the ‘Enable Clock Management- Part 2’ action can be continued. When PLL is not used, this step can be bypassed as shown in Figure 10 on page 13.

Table 6. ENABLE CLOCK MANAGEMENT REGISTER UPLOAD − PART 1

Upload #	Address	Data	Description
8-bit mode with PLL			
1	2	0x0000	Monochrome sensor
		0x0001	Color sensor
2	32	0x200C	Configure clock management
3	20	0x0000	Configure clock management
4	17	0X210F	Configure PLL
5	26	0x1180	Configure PLL lock detector
6	27	0xCCBC	Configure PLL lock detector
7	8	0x0000	Release PLL soft reset
8	16	0x0003	Enable PLL
8-bit mode without PLL			
1	2	0x0000	Monochrome sensor
		0x0001	Color sensor
2	32	0x2008	Configure clock management
3	20	0x0001	Enable LVDS clock input

Table 6. ENABLE CLOCK MANAGEMENT REGISTER UPLOAD – PART 1

Upload #	Address	Data	Description
10-bit mode with PLL			
1	2	0x0000	Monochrome sensor
		0x0001	Color sensor
2	32	0x2004	Configure clock management
3	20	0x0000	Configure clock management
4	17	0x2113	Configure PLL
5	26	0x2280	Configure PLL lock detector
6	27	0x3D2D	Configure PLL lock detector
7	8	0x0000	Release PLL soft reset
8	16	0x0003	Enable PLL
10-bit mode without PLL			
1	2	0x0000	Monochrome sensor
		0x0001	Color sensor
2	32	0x2000	Configure clock management
3	20	0x0001	Enable LVDS clock input

Enable Clock Management - Part 2

The next step to configure the clock management consists of SPI uploads which enables all internal clock distribution. The required uploads are listed in Table 7. Note that it is important to follow the upload sequence listed in Table 7.

Table 7. ENABLE CLOCK MANAGEMENT REGISTER UPLOAD – PART 2

Upload #	Address	Data	Description
8-bit mode with PLL			
1	9	0x0000	Release clock generator soft reset
2	32	0x200E	Enable logic clock
3	34	0x0001	Enable logic blocks
8-bit mode without PLL			
1	9	0x0000	Release clock generator soft reset
2	32	0x200A	Enable logic clock
3	34	0x0001	Enable logic blocks
10-bit mode with PLL			
1	9	0x0000	Release clock generator soft reset
2	32	0x2006	Enable logic clock
3	34	0x0001	Enable logic blocks
10-bit mode without PLL			
1	9	0x0000	Release clock generator soft reset
2	32	0x2002	Enable logic clock
3	34	0x0001	Enable logic blocks

Required Register Upload

In this phase, the ‘reserved’ register settings are uploaded through the SPI register. Different settings are not allowed and may cause the sensor to malfunction. The required uploads are listed in Table 8.

NOTE: This table is subject to change.

Table 8. REQUIRED REGISTER UPLOAD

Upload #	Address	Data	Description
1	41	0x085A	Configure image core
2	129[13]	0x0	10-bit mode
		0x1	8-bit mode
3	65	0x28CB	Configure CP biasing
4	66	0x53C6	Configure AFE biasing
5	67	0x0344	Configure MUX biasing
6	68	0x0085	Configure LVDS biasing
7	70	0x4820	Configure reserved register
8	81	0x86A1	Configure reserved register
9	128	0x460F	Configure black calibration
10	176	0x00F5	Configure AEC
11	180	0x00FD	Configure AEC
12	181	0x0144	Configure AEC
13	218	0x160B	Configure sequencer
14	224	0x3E13	Configure sequencer
15	456	0x0386	Configure sequencer
16	447	0x0BF1	Configure sequencer
17	448	0x0BC3	Configure sequencer

Soft Power Up

During the soft power up action, the internal blocks are enabled and prepared to start processing the image data stream. This action exists of a set of SPI uploads. The soft power up uploads are listed in Table 9.

Table 9. SOFT POWER UP REGISTER UPLOADS FOR MODE DEPENDENT REGISTERS

Upload #	Address	Data	Description
8-bit mode with PLL			
1	32	0x200F	Enable analog clock distribution
2	10	0x0000	Release soft reset state
3	64	0x0001	Enable biasing block
4	72	0x0403	Enable charge pump
5	40	0x0003	Enable column multiplexer
6	48	0x0001	Enable AFE
7	112	0x0007	Enable LVDS transmitters
8-bit mode without PLL			
1	32	0x200B	Enable analog clock distribution
2	10	0x0000	Release soft reset state
3	64	0x0001	Enable biasing block
4	72	0x0403	Enable charge pump
5	40	0x0003	Enable column multiplexer

Table 9. SOFT POWER UP REGISTER UPLOADS FOR MODE DEPENDENT REGISTERS

Upload #	Address	Data	Description
6	48	0x0001	Enable AFE
7	112	0x0007	Enable LVDS transmitters
10-bit mode with PLL			
1	32	0x2007	Enable analog clock distribution
2	10	0x0000	Release soft reset state
3	64	0x0001	Enable biasing block
4	72	0x0403	Enable charge pump
5	40	0x0003	Enable column multiplexer
6	48	0x0001	Enable AFE
7	112	0x0007	Enable LVDS transmitters
10-bit mode without PLL			
1	32	0x2003	Enable analog clock distribution
2	10	0x0000	Release soft reset state
3	64	0x0001	Enable biasing block
4	72	0x0403	Enable charge pump
5	40	0x0003	Enable column multiplexer
6	48	0x0001	Enable AFE
7	112	0x0007	Enable LVDS transmitters

Enable Sequencer

During the ‘Enable Sequencer’ action, the frame grabbing sequencer is enabled. The sensor starts grabbing images in the configured operation mode. Refer to Sensor States on page 12 for an overview of the possible operation modes.

The ‘Enable Sequencer’ action consists of a set of register uploads. The required uploads are listed in Table 10.

Table 10. ENABLE SEQUENCER REGISTER UPLOAD

Upload #	Address	Data	Description
1	192[0]	0x1	Enable sequencer. Note that this address contains other configuration bits to select the operation mode.

User Actions: Functional Modes to Power Down Sequences

Refer to Silicon Errata on page 67 for standby power considerations.

Disable Sequencer

During the ‘Disable Sequencer’ action, the frame grabbing sequencer is stopped. The sensor stops grabbing images and returns to the idle mode.

The ’Disable Sequencer’ action consists of a set of register uploads. as listed in Table 11.

Table 11. DISABLE SEQUENCER REGISTER UPLOAD

Upload #	Address	Data	Description
1	192[0]	0x0	Disable sequencer. Note that this address contains other configuration bits to select the operation mode.

Soft Power Down

During the soft power down action, the internal blocks are disabled and the sensor is put in standby state to reduce the current dissipation. This action exists of a set of SPI uploads. The soft power down uploads are listed in Table 12.

Table 12. SOFT POWER DOWN REGISTER UPLOAD

Upload #	Address	Data	Description
1	112	0x0000	Disable LVDS transmitters
2	48	0x0000	Disable AFE
3	40	0x0000	Disable column multiplexer
4	72	0x0200	Disable charge pump
5	64	0x0000	Disable biasing block
6	10	0x0999	Soft reset

Disable Clock Management - Part 2

The 'Disable Clock Management' action stops the internal clocking to further decrease the power dissipation. This action can be implemented with the SPI uploads as shown in Table 13.

Table 13. DISABLE CLOCK MANAGEMENT REGISTER UPLOAD – PART 2

Upload #	Address	Data	Description
8-bit mode with PLL			
1	34	0x0000	Disable logic blocks
2	32	0x200C	Disable logic clock
3	9	0x0009	Soft reset clock generator
8-bit mode without PLL			
1	34	0x0000	Disable logic blocks
2	32	0x2008	Disable logic clock
3	9	0x0009	Soft reset clock generator
10-bit mode with PLL			
1	34	0x0000	Disable logic blocks
2	32	0x2004	Disable logic clock
3	9	0x0009	Soft reset clock generator

Disable Clock Management - Part 1

The 'Disable Clock Management' action stops the internal clocking to further decrease the power dissipation. This action can be implemented with the SPI uploads as shown in Table 14.

Table 14. DISABLE CLOCK MANAGEMENT REGISTER UPLOAD – PART 1

Upload #	Address	Data	Description
1	16	0x0000	Disable PLL
2	8	0x0099	Soft reset PLL
3	20	0x0000	Configure clock management

Power Down Sequence

Figure 12 illustrates the timing diagram of the preferred power down sequence. It is important that the sensor is in reset before the clock input stops running. Otherwise, the internal PLL becomes unstable and the sensor gets into an unknown state. This can cause high peak currents.

The same applies for the ramp down of the power supplies. The preferred order to ramp down the supplies is first vdd_pix, second vdd_33, and finally vdd_18. Any other sequence can cause high peak currents.

NOTE: The 'clock input' can be the CMOS PLL clock input (clk_pll), or the LVDS clock input (lvds_clock_inn/p) in case the PLL is bypassed.

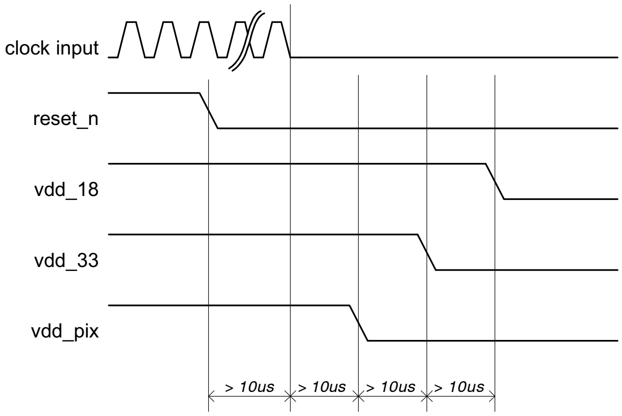


Figure 12. Power Down Sequence

Sensor Reconfiguration

During the standby, idle, or running state several sensor parameters can be reconfigured.

- Frame Rate and Exposure Time: Frame rate and exposure time changes can occur during standby, idle, and running states.
- Signal Path Gain: Signal path gain changes can occur during standby, idle, and running states.
- Windowing: Changes with respect to windowing can occur during standby, idle, and running states. Refer to Multiple Window Readout on page 29 for more information.
- Subsampling: Changes of the subsampling mode can occur during standby, idle, and running states. Refer to Subsampling on page 30 for more information.
- Shutter Mode: The shutter mode can only be changed during standby or idle mode. Reconfiguring the shutter mode during running state is not supported.

Sensor Configuration

This device contains multiple configuration registers. Some of these registers can only be configured while the sensor is not acquiring images (while register 192[0] = 0), while others can be configured while the sensor is acquiring images. For the latter category of registers, it is possible to distinguish the register set that can cause corrupted images (limited number of images containing visible artifacts) from the set of registers that are not causing corrupted images.

These three categories are described here.

Static Readout Parameters

Some registers are only modified when the sensor is not acquiring images. Reconfiguration of these registers while images are acquired can cause corrupted frames or even interrupt the image acquisition. Therefore, it is recommended to modify these static configurations while the sequencer is disabled (register 192[0] = 0). The registers shown in Table 15 should not be reconfigured during image acquisition. A specific configuration sequence applies for these registers. Refer to the operation flow and startup description.

Table 15. STATIC READOUT PARAMETERS

Group	Addresses	Description
Clock generator	32	Configure according to recommendation
Image core	40	Configure according to recommendation
AFE	48	Configure according to recommendation
Bias	64–71	Configure according to recommendation
LVDS	112	Configure according to recommendation
Sequencer mode selection	192 [6:1]	Operation modes are: • Rolling shutter enable • triggered_mode • slave_mode
All reserved registers		Keep reserved registers to their default state, unless otherwise described in the recommendation

Dynamic Configuration Potentially Causing Image Artifacts

The category of registers as shown in Table 16 consists of configurations that do not interrupt the image acquisition process, but may lead to one or more corrupted images during and after the re-configuration. A corrupted image is an image containing visible artifacts. A typical example of a corrupted image is an image which is not uniformly exposed.

The effect is transient in nature and the new configuration is applied after the transient effect.

Table 16. DYNAMIC CONFIGURATION POTENTIALLY CAUSING IMAGE ARTIFACTS

Group	Addresses	Description
Black level configuration	128–129 197[8]	Reconfiguration of these registers may have an impact on the black-level calibration algorithm. The effect is a transient number of images with incorrect black level compensation.
Sync codes	129[13] 130–135	Incorrect sync codes may be generated during the frame in which these registers are modified.
Datablock test configurations	144–150	Modification of these registers may generate incorrect test patterns during a transient frame.

Dynamic Readout Parameters

It is possible to reconfigure the sensor while it is acquiring images. Frame-related parameters are internally resynchronized to frame boundaries, such that the modified parameter does not affect a frame that has already started. However, there can be restrictions to some registers as shown in Table 17. Some reconfiguration may lead to one frame being blanked. This happens when the modification requires more than one frame to settle. The image is blanked out and training patterns are transmitted on the data and sync channels.

Table 17. DYNAMIC READOUT PARAMETERS

Group	Addresses	Description
Subsampling/binning	192[7] 192[8]	Subsampling or binning is synchronized to a new frame start.
Black lines	197	Reconfiguration of these parameters causes one frame to be blanked out in rolling shutter operation mode, as the reset pointers need to be recalculated for the new frame timing. No blanking in global shutter mode
Dummy lines	198	Reconfiguration of these parameters causes one frame to be blanked out in rolling shutter operation mode, as the reset pointers need to be recalculated for the new frame timing. No blanking in global shutter mode.
ROI configuration	195 256–279	Optionally, it is possible to blank out one frame after reconfiguration of the active ROI in rolling shutter mode. Therefore, register 206[8] must be asserted (blank_roi_switch configuration). A ROI switch is only detected when a new window is selected as the active window (reconfiguration of register 195). Reconfiguration of the ROI dimension of the active window does not lead to a frame blank and can cause a corrupted image.
Exposure reconfiguration	199-203	Exposure reconfiguration does not cause artifact. However, a latency of one frame is observed unless reg_seq_exposure_sync_mode is set to ‘1’ in triggered global mode (master).
Gain reconfiguration	204	Gains are synchronized at the start of a new frame. Optionally, one frame latency can be incorporated to align the gain updates to the exposure updates (refer to register 199[13] - gain_lat_comp).

Freezing Active Configurations

Though the readout parameters are synchronized to frame boundaries, an update of multiple registers can still lead to a transient effect in the subsequent images, as some configurations require multiple register uploads. For example, to reconfigure the exposure time in master global mode, both the fr_length and exposure registers need to be updated. Internally, the sensor synchronizes these configurations to frame boundaries, but it is still possible that the reconfiguration of multiple registers spans over two or even more frames. To avoid inconsistent combinations, freeze the active settings while altering the SPI registers by disabling synchronization for the corresponding functionality before reconfiguration. When all registers are uploaded, re-enable the synchronization. The sensor's sequencer then updates its active set of registers and uses them for the coming frames. The freezing of the active set of registers can be programmed in the sync_configuration registers, which can be found at the SPI address 206.

Figure 13 shows a re-configuration that does not use the sync_configuration option. As depicted, new SPI configurations are synchronized to frame boundaries.

With sync_configuration = '1'. Configurations are synchronized to the frame boundaries.

Figure 14 shows the usage of the sync_configuration settings. Before uploading a set of registers, the corresponding sync_configuration is de-asserted. After the upload is completed, the sync_configuration is asserted again and the sensor resynchronizes its set of registers to the coming frame boundaries. As seen in the figure, this ensures that the uploads performed at the end of frame N+2 and the start of frame N+3 become active in the same frame (frame N+4).

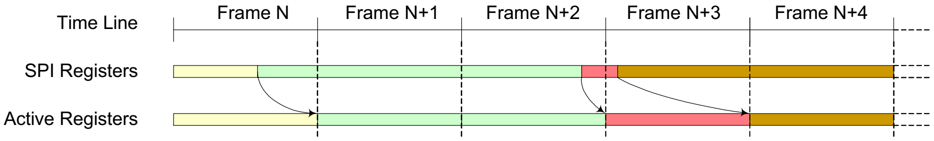


Figure 13. Frame Synchronization of Configurations (no freezing)

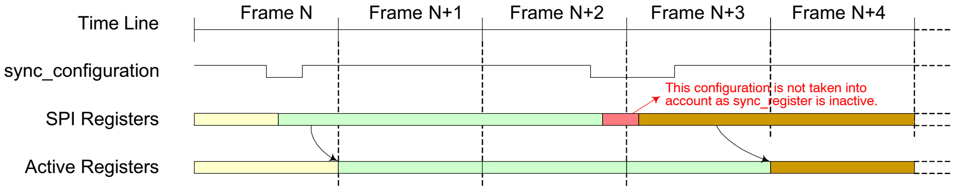


Figure 14. Reconfiguration Using Sync_configuration

NOTE: SPI updates are not taken into account while sync_configuration is inactive. The active configuration is frozen for the sensor. Table 18 lists the several sync_configuration possibilities along with the respective registers being frozen.

Table 18. ALTERNATE SYNC CONFIGURATIONS

Group	Affected Registers	Description
sync_rs_x_length	rs_x_length	Update of x-length configuration (rolling shutter only) is not synchronized at start of frame when '0'. The sensor continues with its previous configurations.
sync_black_lines	black_lines	Update of black line configuration is not synchronized at start of frame when '0'. The sensor continues with its previous configurations.
sync_dummy_lines	dummy_lines	Update of dummy line configuration is not synchronized at start of frame when '0'. The sensor continues with its previous configurations.
sync_exposure	mult_timer fr_length exposure	Update of exposure configurations is not synchronized at start of frame when '0'. The sensor continues with its previous configurations.
sync_gain	mux_gainsw afe_gain	Update of gain configurations is not synchronized at start of frame when '0'. The sensor continues with its previous configurations.
sync_roi	roi_active0[7:0] subsampling binning	Update of active ROI configurations is not synchronized at start of frame when '0'. The sensor continues with its previous configurations. **Note:** The window configurations themselves are not frozen. Re-configuration of active windows is not gated by this setting.

Window Configuration

Global Shutter Mode

Up to 8 windows can be defined in global shutter mode (pipelined or triggered). The windows are defined by registers 256 to 279. Each window can be activated or deactivated separately using register 195. It is possible to reconfigure the windows while the sensor is acquiring images. It is also possible to reconfigure the inactive windows or to switch between predefined windows.

One can switch between predefined windows by reconfiguring the register 195. This way a minimum number of registers need to be uploaded when it is necessary to switch between two or more sets of windows. As an example of this, scanning the scene at higher frame rates using multiple windows and switching to full frame capture when the object is traced. Switching between the two modes only requires an upload of one register.

Rolling Shutter Mode

In rolling shutter mode it is not possible to read multiple windows. Do not activate more than one window (register 195). However, it is possible to configure more than one window and dynamically switch between the different window configurations. Note that switching between two different windows might result in a corrupted frame. This is inherent in the rolling shutter mechanism, where each line must be reset sequentially before being read out. This corrupted window can be blanked out by setting register 206[8]. In this case, a dead time is noted on the LVDS interface when the window-switch occurs in the sensor. During this blank out, training patterns are sent out on the data and sync channels for the duration of one frame.

Black Calibration

The sensor automatically calibrates the black level for each frame. Therefore, the device generates a configurable number of electrical black lines at the start of each frame. The desired black level in the resulting output interface can be configured and is not necessarily targeted to ‘0’. Configuring the target to a higher level yields some information on the left side of the black level distribution, while the other end of the distribution tail is clipped to ‘0’ when setting the black level target to ‘0’.

The black level is calibrated for the 8 columns contained in one kernel. Configurable parameters for the black-level algorithm are listed in Table 19.

Table 19. CONFIGURABLE PARAMETERS FOR BLACK LEVEL ALGORITHM

Group	Addresses	Description
Black Line Generation		
197[7:0]	black_lines	This register configures the number of black lines that are generated at the start of a frame. At least one black line must be generated. The maximum number is 255. **Note:** When the automatic black-level calibration algorithm is enabled, make sure that this register is configured properly to produce sufficient black pixels for the black-level filtering. The number of black pixels generated per line is dependent on the operation mode and window configurations: Global Shutter - Each black line contains 162 kernels. Rolling Shutter - As the line length is fundamental for rolling shutter operation, the length of a black line is defined by the active window.
197[8]	gate_first_line	When asserting this configuration, the first black line of the frame is blanked out and is not used for black calibration. It is recommended to enable this functionality, because the first line can have a different behavior caused by boundary effects. When enabling, the number of black lines must be set to at least two in order to have valid black samples for the calibration algorithm.
Black Value Filtering		
129[0]	auto_blackcal_enable	Internal black-level calibration functionality is enabled when set to ‘1’. Required black level offset compensation is calculated on the black samples and applied to all image pixels. When set to ‘0’, the automatic black-level calibration functionality is disabled. It is possible to apply an offset compensation to the image pixels, which is defined by the registers 129[10:1]. **Note:** Black sample pixels are not compensated; the raw data is sent out to provide external statistics and, optionally, calibrations.
129[9:1]	blackcal_offset	Black calibration offset that is added or subtracted to each regular pixel value when auto_blackcal_enable is set to ‘0’. The sign of the offset is determined by register 129[10] (blackcal_offset_dec). **Note:** All channels use the same offset compensation when automatic black calibration is disabled. The calculated black calibration factors are frozen when this register is set to 0x1FF (all−‘1’) in auto calibration mode. Any value different from 0x1FF re−enables the black calibration algorithm. This freezing option can be used to prevent eventual frame to frame jitter on the black level as the correction factors are recalculated every frame. It is recommended to enable the black calibration regularly to compensate for temperature changes.
129[10]	blackcal_offset_dec	Sign of blackcal_offset. If set to ‘0’, the black calibration offset is added to each pixel. If set to ‘1’, the black calibration offset is subtracted from each pixel. This register is not used when auto_blackcal_enable is set to ‘1’.
128[10:8]	black_samples	The black samples are low-pass filtered before being used for black level calculation. The more samples are taken into account, the more accurate the calibration, but more samples require more black lines, which in turn affects the frame rate. The effective number of samples taken into account for filtering is 2^ black_samples. **Note:** An error is reported by the device if more samples than available are requested (refer to register 136).
Black Level Filtering Monitoring		
136	blackcal_error0	An error is reported by the device if there are requests for more samples than are available (each bit corresponding to one data path). The black level is not compensated correctly if one of the channels indicates an error. There are three possible methods to overcome this situation and to perform a correct offset compensation: • Increase the number of black lines such that enough samples are generated at the cost of increasing frame time (refer to register 197). • Relax the black calibration filtering at the cost of less accurate black level determination (refer to register 128). • Disable automatic black level calibration and provide the offset via SPI register upload. Note that the black level can drift in function of the temperature. It is thus recommended to perform the offset calibration periodically to avoid this drift.

Serial Peripheral Interface

The sensor configuration registers are accessed through an SPI. The SPI consists of four wires:

- sck: Serial Clock
- ss_n: Active Low Slave Select
- mosi: Master Out, Slave In, or Serial Data In
- miso: Master In, Slave Out, or Serial Data Out

The SPI is synchronous to the clock provided by the master (sck) and asynchronous to the sensor's system clock. When the master wants to write or read a sensor's register, it selects the chip by pulling down the Slave Select line (ss_n). When selected, data is sent serially and synchronous to the SPI clock (sck).

Figure 15 shows the communication protocol for read and write accesses of the SPI registers. The VITA 5000 sensor uses 9-bit addresses and 16-bit data words.

Data driven by the system is colored blue in Figure 15, while data driven by the sensor is colored yellow. The data in grey indicates high-Z periods on the miso interface. Red markers indicate sampling points for the sensor (mosi sampling); green markers indicate sampling points for the system (miso sampling during read operations).

The access sequence is:

1. Select the sensor for read or write by pulling down the ss_n line.
2. One SPI clock cycle after selecting the sensor, the 9-bit data is transferred, most significant bit first. The sck clock is passed through to the sensor as indicated in Figure 15. The sensor samples this data on a rising edge of the sck clock (mosi needs to be driven by the system on the falling edge of the sck clock).
3. The tenth bit sent by the master indicates the type of transfer: high for a write command, low for a read command.
4. Data transmission:
   - For write commands, the master continues sending the 16-bit data, most significant bit first.
   - For read commands, the sensor returns the requested address on the miso pin, most significant bit first. The miso pin must be sampled by the system on the falling edge of sck (assuming nominal system clock frequency and maximum 10 MHz SPI frequency).
5. When data transmission is complete, the system deselects the sensor one clock period after the last bit transmission by pulling ss_n high.

Maximum frequency for the SPI depends on the input clock and type of sensor. The frequency is 1/6th of the PLL input clock or 1/30th (in 10-bit mode) and 1/24th (in 8-bit mode) of the LVDS input clock frequency.

At nominal input frequency (62 Mhz / 310 MHz / 248 MHz), the maximum frequency for the SPI is 10 MHz. Bursts of SPI commands can be issued by leaving at least two SPI clock periods between two register uploads. Deselect the chip between the SPI uploads by pulling the ss_n pin high.

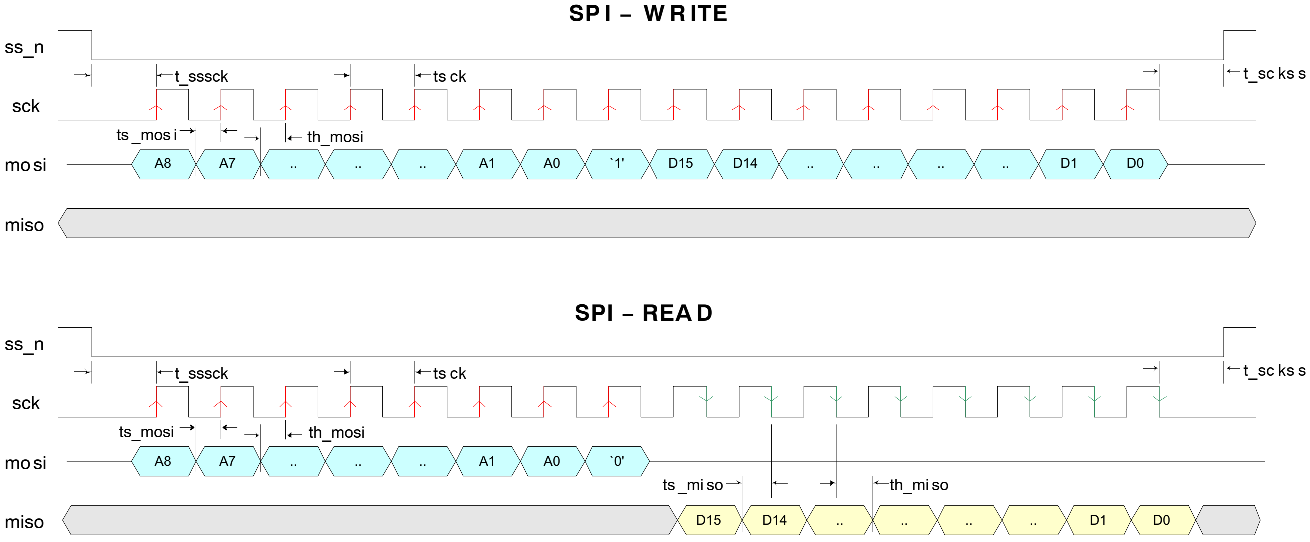


Figure 15. SPI Read and Write Timing Diagram

Table 20. SPI TIMING REQUIREMENTS

Group	Addresses	Description	Units
tsck	sck clock period	100 (*)	ns
tsssck	ss_n low to sck rising edge	tsck	ns
tsckss	sck falling edge to ss_n high	tsck	ns
ts_mosi	Required setup time for mosi	20	ns
th_mosi	Required hold time for mosi	20	ns
ts_miso	Setup time for miso	tsck/2-10	ns
th_miso	Hold time for miso	tsck/2-20	ns
tspi	Minimal time between two consecutive SPI accesses (not shown in figure)	2 x tsck	ns

*Value indicated is for nominal operation. The maximum SPI clock frequency depends on the sensor configuration (operation mode, input clock). tsck is defined as $1/f_{SPI}$. See text for more information on SPI clock frequency restrictions.

IMAGE SENSOR TIMING AND READOUT

The following sections describe the configurations for single slope reset mechanism. Dual and triple slope handling during global shutter operation is similar to the single slope operation. Extra integration time registers are available.

Global Shutter Mode

Pipelined Global Shutter (Master)

The integration time is controlled by the registers fr_length[15:0] and exposure[15:0]. The mult_timer configuration defines the granularity of the registers reset_length and exposure. It is read as number of system clock cycles (16.129 ns nominal at 62 MHz). The exposure control for (Pipelined) Global Master mode is depicted in Figure 16.

The pixel values are transferred to the storage node during FOT, after which all photo diodes are reset. The reset state remains active for a certain time, defined by the reset_length and mult_timer registers, as shown in the figure. Note that meanwhile the image array is read out line by line. After this reset period, the global photodiode reset condition is abandoned. This indicates the start of the integration or exposure time. The length of the exposure time is defined by the registers exposure and mult_timer.

NOTE: The start of the exposure time is synchronized to the start of a new line (during ROT) if the exposure period starts during a frame readout. As a consequence, the effective time during which the image core is in a reset state is extended to the start of a new line.

- Make sure that the sum of the reset time and exposure time exceeds the time required to readout all lines. If this is not the case, the exposure time is extended until all (active) lines are read out.
- Alternatively, it is possible to specify the frame time and exposure time. The sensor automatically calculates the required reset time. This mode is enabled by the fr_mode register. The frame time is specified in the register fr_length.

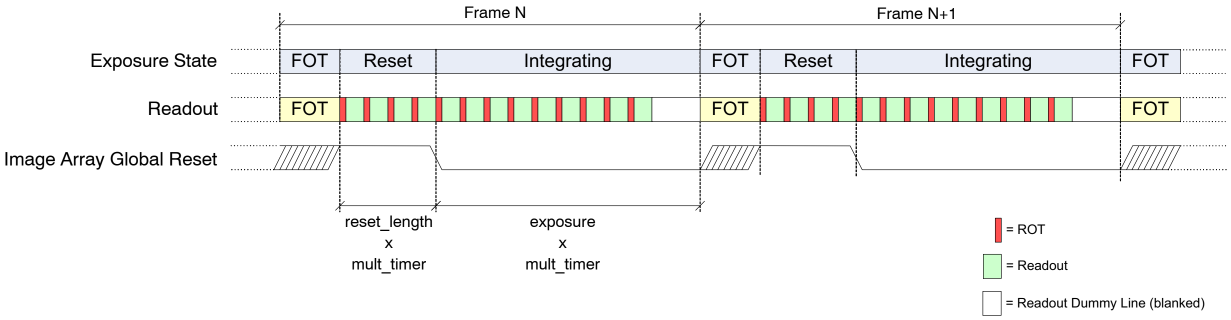


Figure 16. Integration Control for (Pipelined) Global Shutter Mode (Master)

Triggered Global Shutter (Master)

In master triggered global mode, the start of integration time is controlled by a rising edge on the trigger0 pin. The exposure or integration time is defined by the registers exposure and mult_timer, as in the master pipelined global mode. The fr_length configuration is not used. This operation is graphically shown in Figure 17.

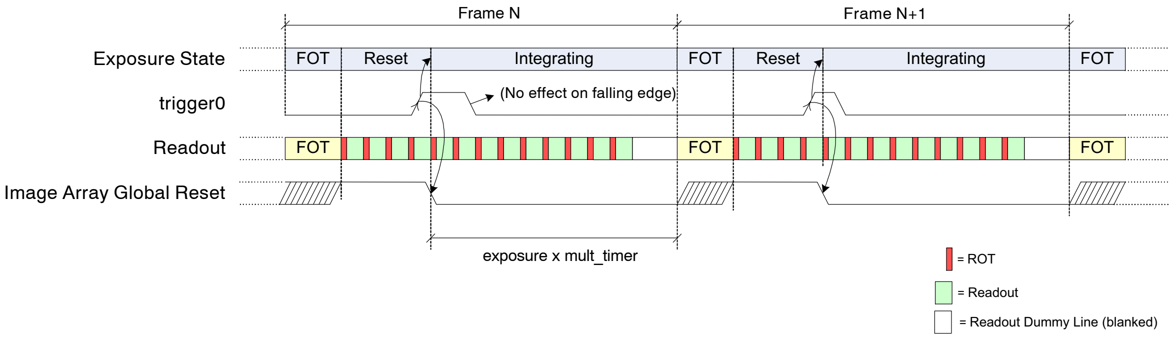


Figure 17. Exposure Time Control in Triggered Global Mode (Master)

Notes:

- The falling edge on the trigger pin does not have any impact. Note however the trigger must be asserted for at least 100 ns.
- The start of the exposure time is synchronized to the start of a new line (during ROT) if the exposure period starts during a frame readout. As a consequence, the effective time during which the image core is in a reset state is extended to the start of a new line.
- If the exposure timer expires before the end of readout, the exposure time is extended until the end of the last active line.
- The trigger pin needs to be kept low during the FOT. The monitor pins can be used as a feedback to the FPGA/controller (eg. use monitor0, indicating the very first line when monitor_select = 0x5 − a new trigger can be initiated after a rising edge on monitor0).

Triggered Global Shutter (Slave)

Exposure or integration time is fully controlled by means of the trigger pin in slave mode. The registers fr_length, exposure and mult_timer are ignored by the sensor.

A rising edge on the trigger pin indicates the start of the exposure time, while a falling edge initiates the transfer to the pixel storage node and readout of the image array. In other words, the high time of the trigger pin indicates the integration time, the period of the trigger pin indicates the frame time.

The use of the trigger during slave mode is shown in Figure 18.

Notes:

- The registers exposure, fr_length, and mult_timer are not used in this mode.
- The start of exposure time is synchronized to the start of a new line (during ROT) if the exposure period starts during a frame readout. As a consequence, the effective time during which the image core is in a reset state is extended to the start of a new line.
- If the trigger is de-asserted before the end of readout, the exposure time is extended until the end of the last active line.
- The trigger pin needs to be kept low during the FOT. The monitor pins can be used as a feedback to the FPGA/controller (eg. use monitor0, indicating the very first line when monitor_select = 0x5 − a new trigger can be initiated after a rising edge on monitor0).

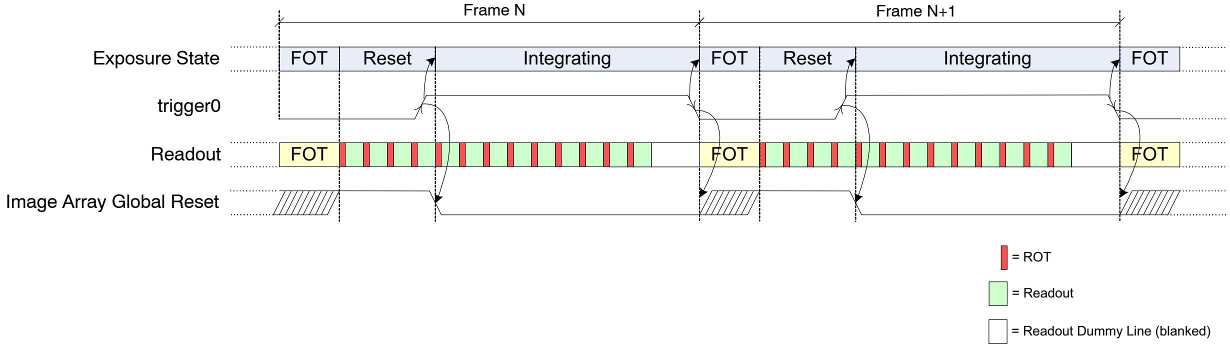


Figure 18. Exposure Time Control in Global−Slave Mode

Rolling Shutter Mode

The exposure time during rolling shutter mode is always an integer multiple of line-times. The exposure time is defined by the register exposure and expressed in number of lines. The register fr_length and mult_timer are not used in this mode.

The maximum exposure time is limited by the frame time. It is possible to increase the exposure time at the cost of the frame rate by adding so called dummy lines. A dummy line lasts for the same time as a regular line, but no pixel data is transferred to the system. The number of dummy lines is controlled by the register dummy_lines. The rolling shutter exposure mechanism is graphically shown in Figure 19.

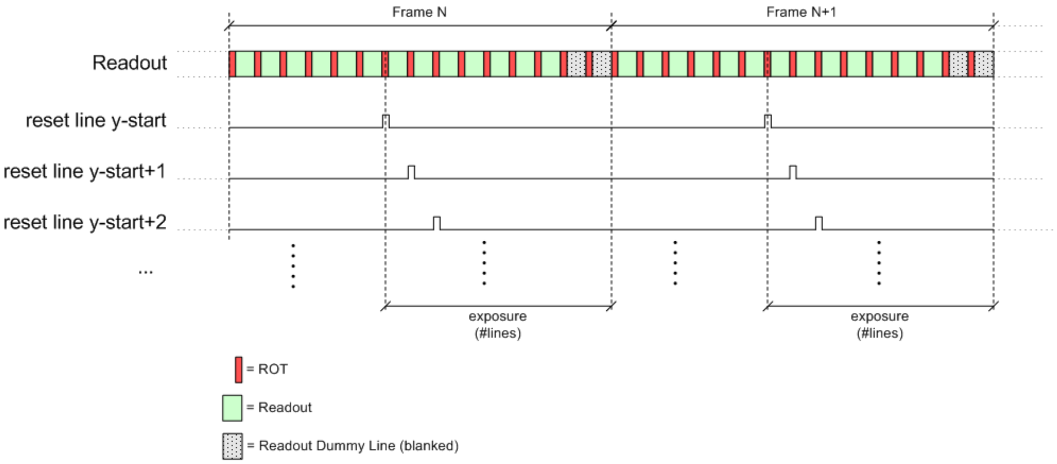


Figure 19. Integration Control in Rolling Shutter Mode

Note:

The duration of one line is the sum of the ROT and the time required to read out one line (depends on the number of active kernels in the window). Optionally, this readout time can be extended by the configuration rs_x_length. This register, expressed in number of periods of the logic clock (16.129 ns for the V1-SN/SE version and 64.516 ns for the V2-SN/SE version), determines the length of the x-readout. However, the minimum for rs_x_length is governed by the window size (x-size).

It is clear that when the number of rows and/or the length of a row are reduced (by windowing or subsampling), the frame time decreases and consequently the frame rate increases.

To be able to artificially increase the frame time, it is possible to:

- add dummy clock cycles to a row time
- add dummy rows to the frame

ADDITIONAL FEATURES

Multiple Window Readout

The VITA 5000 sensor supports multiple window readout, which means that only the user-selected Regions Of Interest (ROI) are read out. This allows limiting data output for every frame, which in turn allows increasing the frame rate.

- In global shutter mode, up to eight ROIs can be configured.
- In rolling shutter mode, only a single ROI is supported. All multiple windowing features described further in this section are only valid for global shutter mode.

Window Configuration

Figure 20 shows the four parameters defining a region of interest (ROI).

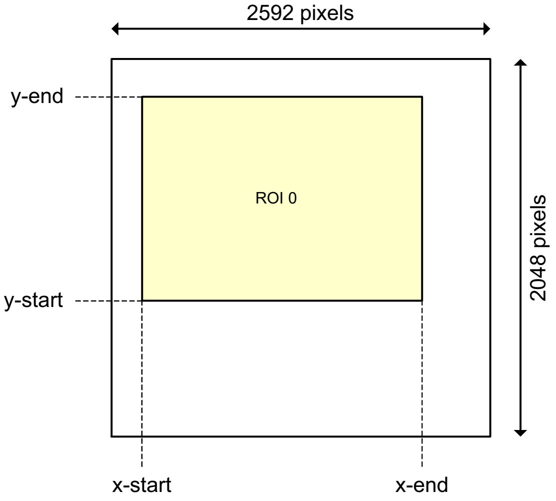


Figure 20. Region of Interest Configuration

- x−start[7:0]

x-start defines the x-starting point of the desired window. The sensor reads out 16 pixels in one single clock cycle. As a consequence, the granularity for configuring the x-start position is also 16 pixels for no sub sampling. The value configured in the x-start register is multiplied by 16 to find the corresponding column in the pixel array.

- x-end[7:0]

This register defines the window end point on the x-axis. Similar to x-start, the granularity for this configuration is one kernel. x-end needs to be larger than x-start.

- y-start[10:0]

The starting line of the readout window. The granularity of this setting is one line, except with color sensors where it needs to be an even number.

- y-end[10:0]

The end line of the readout window. y-end must be configured larger than y-start. This setting has the same granularity as the y-start configuration.

Up to eight windows can be defined, possibly (partially) overlapping, as illustrated in Figure 21.

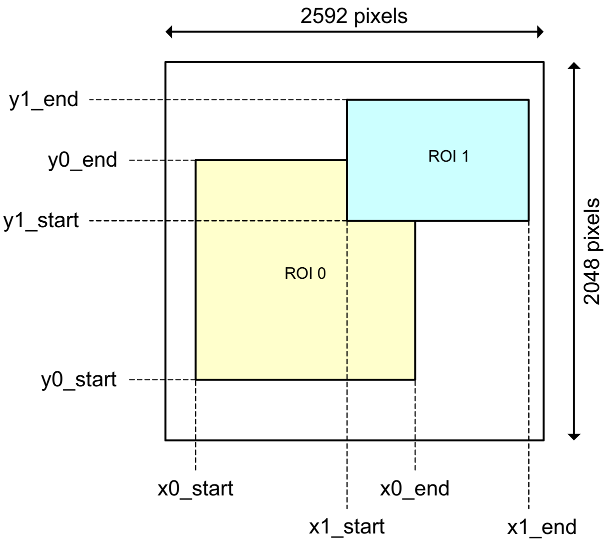


Figure 21. Overlapping Multiple Window Configuration

The sequencer analyses each line that need to be read out for multiple windows.

Restrictions

The following restrictions for each line are assumed for the user configuration:

- Windows are ordered from left to right, based on their x−start address:

$$x\_start\_roi(i) \le x\_start\_roi(j)\ AND$$

$$x\_end\_roi(i) \le x\_end\_roi(j)$$

$$\text{Where } j > i$$

Processing Multiple Windows

The sequencer control block houses two sets of counters to construct the image frame. As previously described, the y-counter indicates the line that needs to be read out and is incremented at the end of each line. For the start of the frame, it is initialized to the y-start address of the first window and it runs until the y-end address of the last window to be read out. The last window is configured by the configuration registers and it is not necessarily window #7.

The x-counter starts counting from the x-start address of the window with the lowest ID which is active on the addressed line. Only windows for which the current y-address is enclosed are taken into account for scanning. Other windows are skipped.

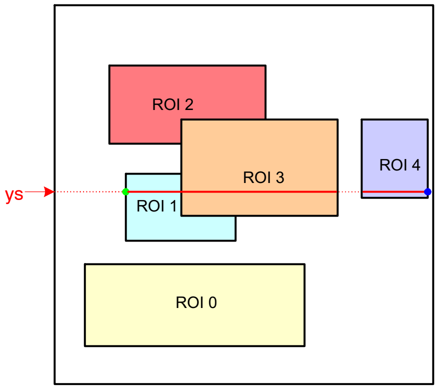


Figure 22. Scanning the Image Array with Five Windows

Figure 22 illustrates a practical example of a configuration with five windows. The current position of the read pointer (ys) is indicated by a red line crossing the image array. For this position of the read pointer, three windows need to be read out. The initial start position for the x-kernel pointer is the x-start configuration of ROI1. Kernels are scanned up to the ROI3 x-end position. From there, the x-pointer jumps to the next window, which is ROI4 in this illustration. When reaching ROI4's x-end position, the read pointer is incremented to the next line and xs is reinitialized to the starting position of ROI1.

Notes:

- The starting point for the readout pointer at the start of a frame is the y-start position of the first active window.
- The read pointer is not necessarily incremental by one, but depending on the configuration, it can jump in y-direction. In Figure 22, this is the case when reaching the end of ROI0 where the read pointer jumps to the y-start position of ROI1
- The x-pointer starting position is equal to the x-start configuration of the first active window on the current line addressed. This window is not necessarily window #0.
- The x-pointer is not necessarily incremented by one each cycle. At the end of a window it can jump to the start of the next window.
- Each window can be activated separately. There is no restriction on which window and how many of the 8 windows are active.

Subsampling

Subsampling is used to reduce the image resolution. This allows increasing the frame rate. Two subsampling modes are supported: for monochrome sensors (V1SN) and color sensors (V1SE).

Monochrome Sensors

For monochrome sensors, the read-1-skip-1 subsampling scheme is used. Subsampling occurs both in x- and y-direction.

Color Sensors

For color sensors, the read-2-skip-2 subsampling scheme is used. Subsampling occurs both in x- and y- direction. Figure 23 shows which pixels are read and which ones are skipped.

Binning

Pixel binning is a technique in which different pixels are averaged in the analog domain. A 2x1 binning mode is available on the monochrome sensors. When enabled, two neighboring pixels in the x-direction are averaged while line readout happens in a read-1-skip-1 manner.

Pixel binning is not supported on color sensors.

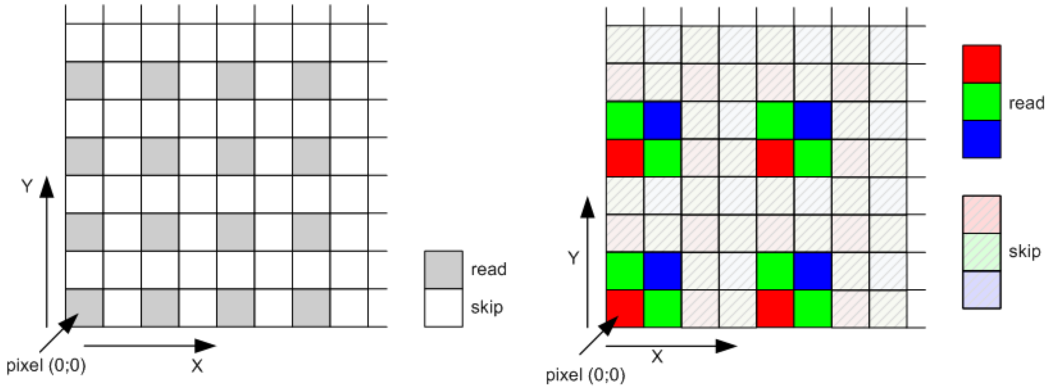


Figure 23. Subsampling Scheme for Monochrome and Color Sensors

Multiple Slope Integration

'Multiple Slope Integration' is a method to increase the dynamic range of the sensor. The VITA 5000 supports up to three slopes.

Figure 24 shows the sensor response to light when the sensor is used with one slope, two slopes, and three slopes. The X-axis represents the light power; the Y-axis shows the sensor output signal. The kneepoint of the multiple slope curves are adjustable in both position and voltage level.

It is clear that when using only one slope (red curve), the sensor has the same responsivity over the entire range, until the output saturates at the point indicated with 'single slope saturation point'.

To increase the dynamic range of the sensor, a second slope is applied in the dual slope mode (green curve). The sensor has the same responsivity in the black as for a single slope, but from 'knee point 1' on, the sensor is less responsive to incoming light. The result is that the saturation point is at a higher light power level.

To further increase the dynamic range, a third slope can be applied, resulting in a second knee point.

The multiple slope function is only available in global shutter modes. Refer to section Global Shutter Mode on page 26 for general notes applicable to the global shutter operation and more particular to the use of the trigger0 pin.

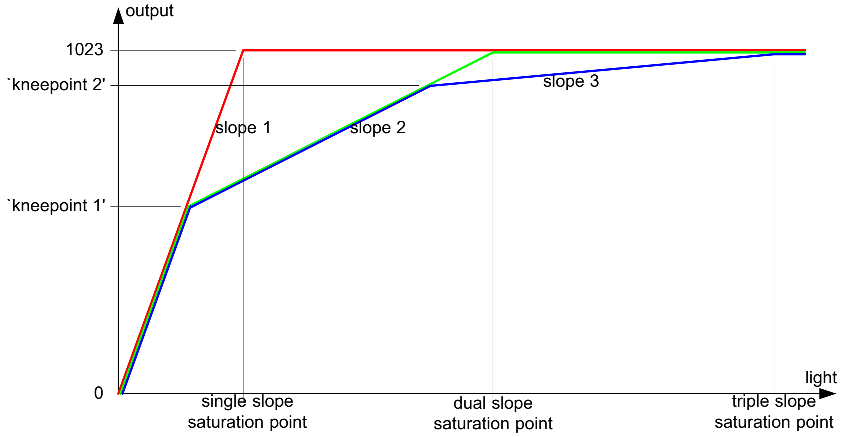


Figure 24. Multiple Slope Operation

Required Register Uploads

Multiple slope integration requires the uploads as described in the following table. Note that these are cumulative with the required register uploads (Table 8). These register uploads are subject to change.

Table 21. REQUIRED UPLOADS FOR MULTIPLE SLOPE INTEGRATION

Upload #	Address	Data	Description
1	421	0x7030	Configure sequencer
2	429	0x7050	Configure sequencer

Kneepoint Configuration (Multiple Slope Reset Levels)

The kneepoint reset levels are configured by means of DAC configurations in the image core. The dual slope kneepoint is configured with the *dac_ds* configuration, while the triple slope kneepoint is configured with the *dac_ts* register setting. Both are located on address 41.

Multiple Slope Integration in Master Mode (Pipelined or Triggered)

In master mode, the time stamps for the double and triple slope resets are configured in a similar way as the exposure time. They are enabled through the registers *dual_slope_enable* and *triple_slope_enable* and their values are defined by the registers *exposure_ds* and *exposure_ts*.

NOTE: Dual and triple slope sequences must start after readout of the previous frame is fully completed.

Figure 25 shows the frame timing for pipelined master mode with dual and triple slope integration and fr_mode = '0' (fr_length representing the reset length).

In triggered master mode, the start of integration is initiated by a rising edge on *trigger0*, while the falling edge does not have any relevance. Exposure duration and dual/triple slope points are defined by the registers.

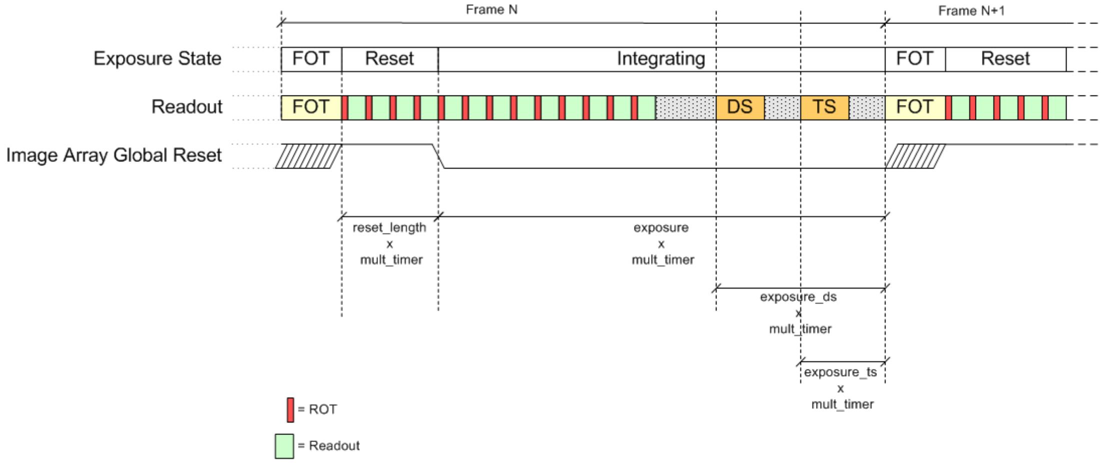


Figure 25. Multiple Slope Operation in Master Mode for fr_mode = ‘0’ (Pipelined)

Slave Mode

In slave mode, the register settings for integration control are ignored. The user has full control through the *trigger0, trigger1* and *trigger2* pins. A falling edge on *trigger1* initiates the dual slope reset while a falling edge on *trigger2* initiates the triple slope reset sequence. Rising edges on *trigger1* and *trigger2* do not have any impact.

NOTE: Dual and triple slope sequences must start after readout of the previous frame is fully completed.

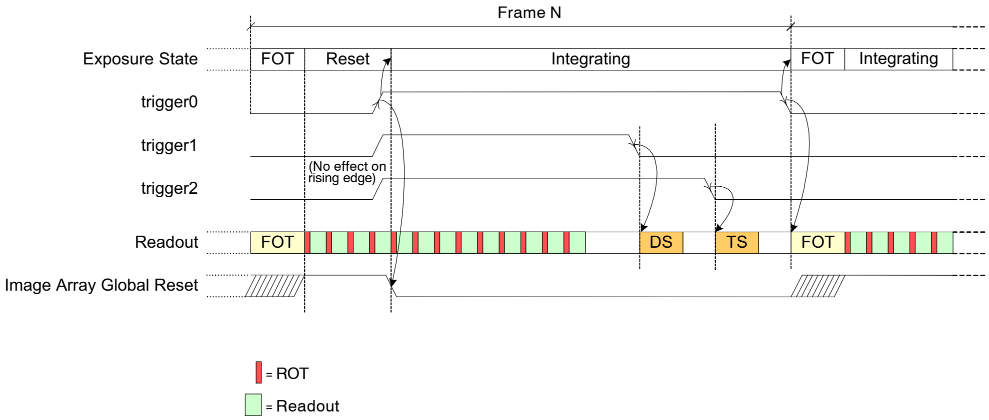


Figure 26. Multiple Slope Operation in Slave Mode

Black Reference

The sensor reads out one or more black lines at the start of every new frame. The number of black lines to be generated is programmable and is minimal equal to 1. The length of the black lines depends on the operation mode: for Rolling Shutter mode, the length of the black line is equal to the line length configured in the active window. For Global Shutter mode, the sensor always reads out the entire line (162 kernels), independent of window configurations.

The black references are used to perform black calibration and offset compensation in the data channels. The raw black pixel data is transmitted over the usual output interface, while the regular image data is compensated (can be bypassed).

On the output interface, black lines can be seen as a separate window, however without Frame Start and Ends (only Line Start/End). The Sync code following the Line Start and Line End indications (“window ID”) contains the active window number for Rolling Shutter operation, while it is 0 for Snapshot Shutter operation. Black reference data is classified by a BL code.

Signal Path Gain

Analog Gain Stages

Two gain steps are available in the analog data path to apply gain to the analog signal before it is digitized. The gain amplifier can apply a gain of 1x to 8x to the analog signal.

The moment a gain re-configuration is applied and becomes valid can be controlled by the gain_lat_comp configuration.

With ‘gain_lat_comp’ set to ‘0’, the new gain configurations are applied from the very next frame.

With ‘gain_lat_comp’ set to ‘1’, the new gain settings are postponed by one extra frame. This feature is useful when exposure time and gain are reconfigured together, as an exposure time update always has one frame latency.

Table 22. SIGNAL PATH GAIN STAGES
(Analog Gain Stages)

gain_stage1	Gain Stage 1	gain_stage2	Gain Stage 2	GAIN total
0x2	1.00	0xF	1.00	1.00
0x2	1.00	0x7	1.14	1.14
0x2	1.00	0x3	1.33	1.33
0x2	1.00	0x5	1.60	1.60
0x2	1.00	0x1	2.00	2.00
0x1	2.00	0x7	1.14	2.29
0x1	2.00	0x3	1.33	2.67
0x1	2.00	0x5	1.60	3.20
0x1	2.00	0x1	2.00	4.00
0x1	2.00	0x6	2.67	5.33
0x1	2.00	0x2	4.00	8.00

Digital Gain Stage

The digital gain stage allows fine gain adjustments on the digitized samples. The gain configuration is an absolute 5.7 unsigned number (5 digits before and 7 digits after the decimal point).

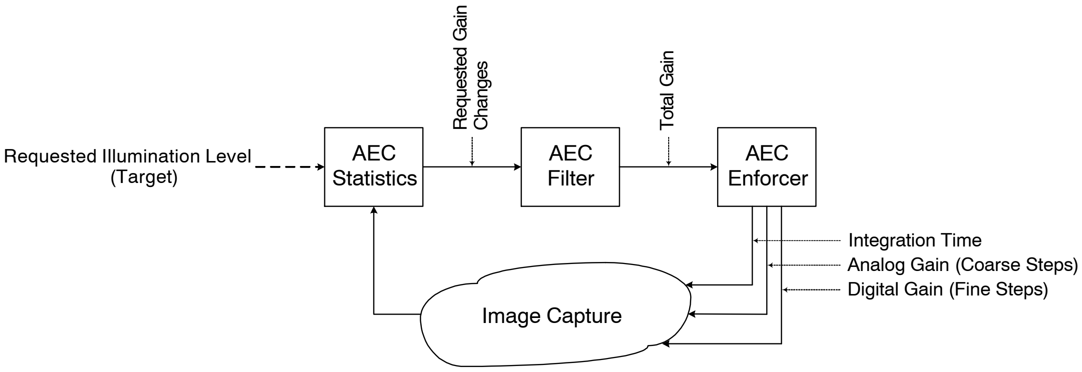


Figure 27. Automatic Exposure Control Loop

Automatic Exposure Control

The exposure control mechanism has the shape of a general feedback control system. Figure 27 shows the high level block diagram of the exposure control loop.

Three main blocks can be distinguished:

- The statistics block compares the average of the current image’s samples to the configured target value for the average illumination of all pixels
- The relative gain change request from the statistics block is filtered in the time domain (low pass filter) before being integrated. The output of the filter is the total requested gain in the complete signal path.
- The enforcer block accepts the total requested gain and distributes this gain over the integration time and gain stages (both analog and digital)

The automatic exposure control loop is enabled by asserting the aec_enable configuration in register 160.

NOTE: Dual and Triple slope integration is not supported in conjunction with the AEC.

AEC Statistics Block

The statistics block calculates the average illumination of the current image. Based on the difference between the calculated illumination and the target illumination the statistics block requests a relative gain change.

Statistics Subsampling and Windowing

For average calculation, the statistics block will sub-sample the current image or windows by taking every fourth sample into account. Note that only the pixels read out through the active windows are visible for the AEC. In the case where multiple windows are active, the samples will be selected from the total samples. Samples contained in a region covered by multiple (overlapping) window will be taking into account only once.

It is possible to define an AEC specific sub-window on which the AEC will calculate it’s average. For instance, the sensor can be configured to read out a larger frame, while the illumination is measured on a smaller region of interest, e.g. center weighted.

Table 23. AEC SAMPLE SELECTION

Register	Name	Description
192[10]	roi_aec_enable	When 0x0, all active windows are selected for statistics calculation. When 0x1, the AEC samples are selected from the active pixels contained in the region of interest defined by roi_aec
253-255	roi_aec	These registers define a window from which the AEC samples will be selected when roi_aec_enable is asserted. Configuration is similar to the regular region of interests. The intersection of this window with the active windows define the selected pixels. It is important that this window at least overlaps with one or more active windows.

Important note for rolling shutter operation: a minimum of 4 dummy lines is required when using the automatic exposure controller.

Target Illumination

The target illumination value is configured by means of register *desired_intensity.*

Table 24. AEC TARGET ILLUMINATION CONFIGURATION

Register	Name	Description
161[9:0]	desired_intensity	Target intensity value, on 10-bit scale. For 8-bit mode, target value is configured on desired_intensity[9:2]

Color Sensor

The weight of each color can be configured for color sensors by means of scale factors. Note these scale factor are only used to calculate the statistics in order to compensate for (off-chip) white balancing and/or color matrices. The pixel values itself are not modified.

The scale factors are configured as 3.7 unsigned numbers (0x80 = unity).

Table 25. COLOR SCALE FACTORS

Register	Name	Description
162[9:0]	red_scale_factor	Red scale factor for AEC statistics
163[9:0]	green1_scale_factor	Green1 scale factor for AEC statistics
164[9:0]	green2_scale_factor	Green2 scale factor for AEC statistics
165[9:0]	blue_scale_factor	Blue scale factor for AEC statistics

Configure these factors to their default value for monochrome sensors.

AEC Filter Block

The filter block low-pass filters the gain change requests received from the statistics block.

The filter can be restarted by asserting the restart_filter configuration of register 160.

AEC Enforcer Block

The enforcer block calculates the four different gain parameters, based on the required total gain, thereby respecting a specific hierarchy in those configurations. Some (digital) hysteresis is added so that the (analog) sensor settings don't need to change too often.

Exposure Control Parameters

The several gain parameters are described below, in the order in which these are controlled by the AEC for large adjustments. Small adjustments are regulated by digital gain only.

- Exposure Time

In rolling shutter mode, the exposure time is the time elapsed between resetting a particular line and reading it out. This time is constant for all lines in a frame, lest the image be non-uniformly exposed. The exposure time is always an integer multiple of the line time.

In a snapshot shutter mode, the exposure is the time between the global image array reset de-assertion and the pixel charge transfer. The granularity of the integration time steps is configured by the *mult_timer* register.

NOTE: The *exposure_time* register is ignored when the AEC is enabled. The register *fr_length* defines the frame time and needs to be configured accordingly.

- Analog Gain

The sensor has two analog gain stages, configurable independently from each other. Typically the AEC shall first regulate the first stage. Optionally this behavior can be inverted by setting the *amp_pri* register.

- Digital Gain

The last gain stage is a gain applied on the digitized samples. The digital gain is represented by a 5.7 unsigned number (i.e. 7 bits after the decimal point). While the analog gain steps are coarse, the digital gain stage makes it possible to achieve very fine adjustments.

AEC Control Range

The control range for each of the exposure parameters can be pre-programmed in the sensor. Note that for rolling shutter operation the maximum integration time should not exceed the number of lines read out (i.e. the sum of black lines, active window-defined lines and dummy lines). Table 26 lists the relevant registers.

Table 26. MINIMUM AND MAXIMUM EXPOSURE CONTROL PARAMETERS

Register	Name	Description
168[15:0]	min_exposure	Lower bound for the integration time applied by the AEC
169[1:0]	min_mux_gain	Lower bound for the first stage analog amplifier. This stage has two configurations with the following approximative gains: 0x0 = 1x 0x1 = 2x
169[3:2]	min_afe_gain	Lower bound for the second stage analog amplifier This stage has four configurations with the following approximative gains: 0x0 = 1.00x 0x1 = 1.33x 0x2 = 2.00x 0x3 = 2.50x
169[15:4]	min_digital_gain	Lower bound for the digital gain stage. This configuration specifies the effective gain in 5.7 unsigned format
170[15:0]	max_exposure	Upper bound for the integration time applied by the AEC
171[1:0]	max_mux_gain	Upper bound for the first stage analog amplifier. This stage has two configurations with the following approximative gains: 0x0 = 1x 0x1 = 2x
171[3:2]	max_afe_gain	Upper bound for the second stage analog amplifier This stage has four configurations with the following approximative gains: 0x0 = 1.00x 0x1 = 1.33x 0x2 = 2.00x 0x3 = 2.50x
171[15:4]	max_digital_gain	Upper bound for the digital gain stage. This configuration specifies the effective gain in 5.7 unsigned format

AEC Update Frequency

As an integration time update has a latency of one frame, the exposure control parameters are evaluated and updated every other frame.

NOTE: The gain update latency must be postpone to match the integration time latency. This is done by asserting the *gain_lat_comp* register on address 204[13].

Exposure Control Status Registers

Configured integration and gain parameters are reported to the user by means of status registers. The sensor provides two levels of reporting: the status registers reported in the AEC address space are updated once the parameters are recalculated and requested to the internal sequencer. The status registers residing in the sequencer's address space on the other hand are updated once these parameters are taking effect on the image readout. The first set shall thus lead the second set of status registers.

Table 27. EXPOSURE CONTROL STATUS REGISTERS

Register	Name	Description
AEC Status Registers		
184[15:0]	total_pixels	Total number of pixels taken into account for the AEC statistics.
186[9:0]	average	Calculated average illumination level for the current frame.
187[15:0]	exposure	AEC calculated exposure. Note: this parameter is updated at the frame end.
188[1:0]	mux_gain	AEC calculated analog gain (1st stage) Note: this parameter is updated at the frame end.
188[3:2]	afe_gain	AEC calculated analog gain (2st stage) Note: this parameter is updated at the frame end.
188[15:4]	digital_gain	AEC calculated digital gain (5.7 unsigned format) Note: this parameter is updated at the frame end.
Sequencer Status Registers		
208[15:0]	mult_timer	mult_timer for current frame (global shutter only). Note: this parameter is updated once it takes effect on the image.
209[15:0]	reset_length	Image array reset length for the current frame (global shutter only). Note: this parameter is updated once it takes effect on the image.
210[15:0]	exposure	Exposure for the current frame. Note: this parameter is updated once it takes effect on the image.
211[15:0]	exposure_ds	Dual slope exposure for the current frame. Note this parameter is not controlled by the AEC. Note: this parameter is updated once it takes effect on the image.
212[15:0]	exposure_ts	Triple slope exposure for the current frame. Note this parameter is not controlled by the AEC. Note: this parameter is updated once it takes effect on the image.

213[4:0]	mux_gainsw	1st stage analog gain for the current frame. Note: this parameter is updated once it takes effect on the image.
213[12:5]	afe_gain	2nd stage analog gain for the current frame. Note: this parameter is updated once it takes effect on the image.
214[11:0]	db_gain	Digital gain configuration for the current frame (5.7 unsigned format). Note: this parameter is updated once it takes effect on the image.
214[12]	dual_slope	Dual slope configuration for the current frame **Note 1**: this parameter is updated once it takes effect on the image. **Note 2**: This parameter is not controlled by the AEC.
214[13]	triple_slope	Triple slope configuration for the current frame. **Note 1**: this parameter is updated once it takes effect on the image. **Note 2**: This parameter is not controlled by the AEC.

Temperature Sensor

The VITA 5000 has an on-chip temperature sensor which can output a digital code (Tsensor) of the silicon junction temperature. The Tsensor output is a 8-bit digital count between 0 and 255, proportional to the temperature of the silicon substrate. This reading can be translated directly to a temperature reading in °C by calibrating the 8-bit readout at 0°C and 70°C to achieve an output accuracy of ±2°C. The Tsensor output can also be calibrated using a single temperature point (example: room temperature or the ambient temperature of the application), to achieve an output accuracy of ±5°C.

The resolution of the temperature sensor in ºC / bit is made almost constant over process variations by design. Therefore any process variation will result in an offset in the bit count and this offset will remain within ±5°C over the temperature range of 0°C and 70°C.

Tsensor output digital code can be read out through the SPI interface. Refer to the Register Map on page 44.

The output of the temperature sensor to the SPI:

tempd_reg_temp<7:0>: This is the 8-bit N count readout proportional to temperature.

The input from the SPI:

The *reg_tempd_enable* is a global enable and this enables or disables the temperature sensor when logic high or logic low respectively. The temperature sensor is reset or disabled when the input *reg_tempd_enable* is set to a digital low state.

Calibration using one temperature point

The temperature sensor resolution is fixed for a given type of package for the operating range of 0°C to +70°C and hence devices can be calibrated at any ambient temperature of the application, with the device configured in the mode of operation.

Interpreting the actual temperature for the digital code readout:

The formula used is

$$\mathbf{T_J = R\ (Nread - Ncalib) + Tcalib}$$

T_J = junction die temperature

R = resolution in degrees/LSB (typical 0.75 deg/LSB)

Nread = Tsensor output (LSB count between 0 and 255)

Tcalib = Tsensor calibration temperature

Ncalib = Tsensor output reading at Tcalib

Monitor Pins

The internal sequencer has two monitor outputs (Pin 44 and Pin 45) that can be used to communicate the internal states from the sequencer. A three-bit register configures the assignment of the pins.

Table 28. REGISTER SETTING FOR THE MONITOR SELECT PIN

monitor_select [2:0] 192 [13:11]	monitor pin	Description
0x0	monitor0 monitor1	‘0’ ‘0’
0x1	monitor0 monitor1	Integration Time ROT Indication (‘1’ during ROT, ‘0’ outside)
0x2	monitor0 monitor1	Integration Time Dual/Triple Slope Integration (asserted during DS/TS FOT sequence)
0x3	monitor0 monitor1	Start of x-Readout Indication Black Line Indication (‘1’ during black lines, ‘0’ outside)
0x4	monitor0 monitor1	Frame Start Indication Start of ROT Indication
0x5	monitor0 monitor1	First Line Indication (‘1’ during first line, ‘0’ for all others) Start of ROT Indication

Table 28. REGISTER SETTING FOR THE MONITOR SELECT PIN

monitor_select [2:0] 192 [13:11]	monitor pin	Description
0x6	monitor0 monitor1	ROT Indication ('1' during ROT, '0' outside) Start of X-Readout Indication
0x7	monitor0 monitor1	Start of X-readout Indication for Black Lines Start of X-readout Indication for Image Lines

DATA OUTPUT FORMAT

The VITA 5000 is available with a LVDS output interface.

- Eight LVDS output channels, together with an LVDS clock output and an LVDS synchronization output channel.

LVDS Interface Version

LVDS Output Channels

The image data output occurs through eight LVDS data channels. A synchronization LVDS channel and an LVDS output clock signal is utilized to synchronize the data.

The eight data channels are used to output the image data only. The sync channel transmits information about the data sent over these data channels (includes codes indicating black pixels, normal pixels, and CRC codes).

8-bit / 10-bit Mode

The sensor can be used in 8-bit or 10-bit mode.

In 10-bit mode, the words on data and sync channel have a 10-bit length. The output data rate is 620 Mbps.

In 8-bit mode, the words on data and sync channel have an 8-bit length, the output data rate is 496 Mbps.

Note that the 8-bit mode can only be used to limit the data rate at the consequence of image data word depth. It is not supported to operate the sensor in 8-bit mode at a higher clock frequency to achieve higher frame rates.

Frame Format

The frame format is explained by example of the readout of two (overlapping) windows as shown in Figure 28 (a).

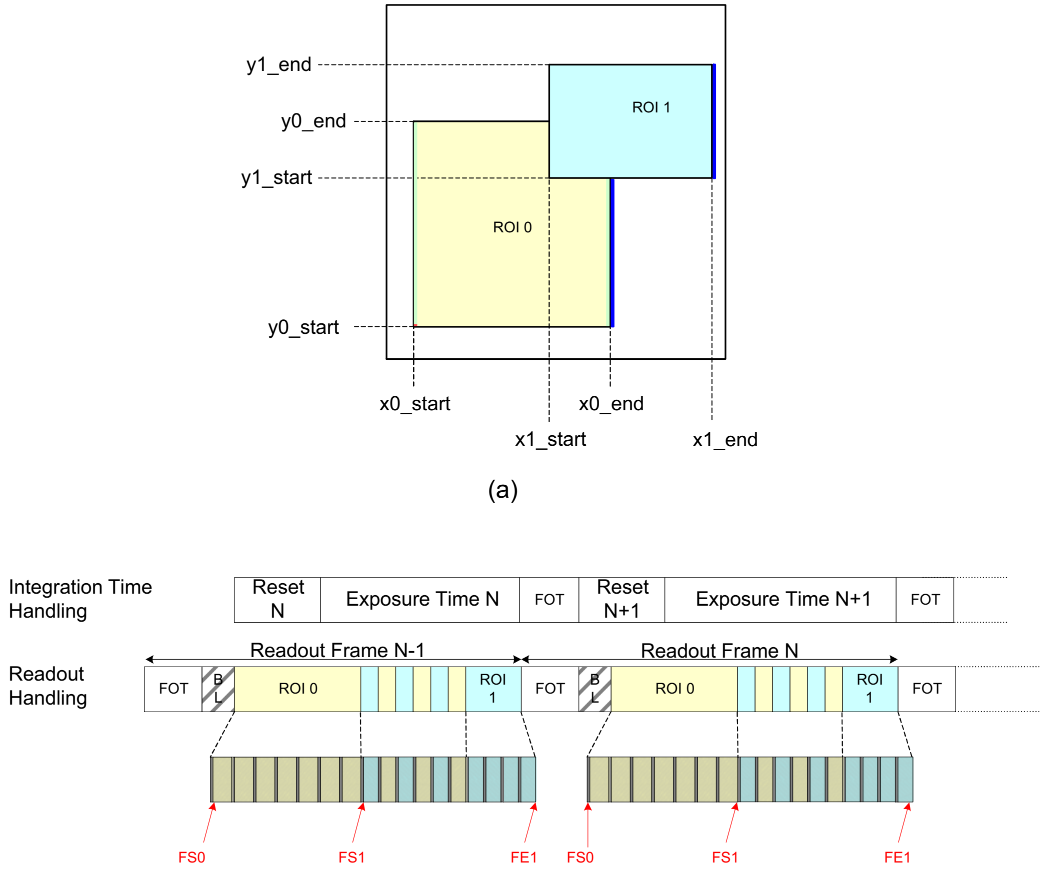
The readout of a frame occurs on a line-by-line basis. The read pointer goes from left to right, bottom to top.

Figure 28 indicates that, after the FOT is completed, the sensor reads out a number of black lines for black calibration purposes. After these black lines, the windows are processed. First a number of lines which only includes information of 'ROI 0' are sent out, starting at position y0_start. When the line at position y1_start is reached, a number of lines containing data of 'ROI 0' and 'ROI 1' are sent out, until the line position of y0_end is reached. From there on, only data of 'ROI 1' appears on the data output channels until line position y1_end is reached.

During read out of the image data over the data channels, the sync channel sends out frame synchronization codes which give information related to the image data that is sent over the eight data output channels.

Each line of a window starts with a Line Start (LS) indication and ends with a Line End (LE) indication. The line start of the first line is replaced by a Frame Start (FS); the line end of the last line is replaced with a Frame End indication (FE). Each such frame synchronization code is followed by a window ID (range 0 to 7). For overlapping windows, the line synchronization codes of the overlapping windows with lower IDs are not sent out (as shown in the illustration: no LE/FE is transmitted for the overlapping part of window 0).

NOTE: In Figure 28, only Frame Start and Frame End Sync words are indicated in (b). CRC codes are also omitted from the figure.



(a)

(b)

Figure 28. V1−SN/SE: Frame Sync Codes

Figure 29 shows the detail of a black line readout during global or full-frame readout.

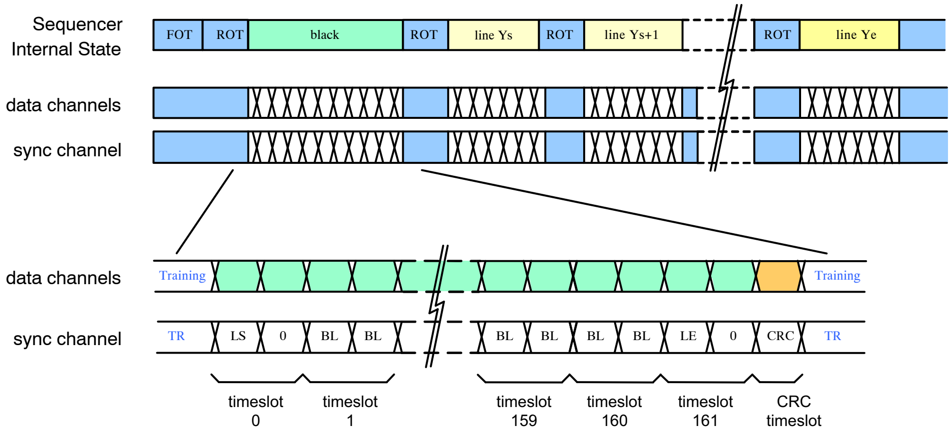


Figure 29. Time Line for Black Line Readout

Figure 30 shows the details of the readout of a number of lines for single window readout, at the beginning of the frame.

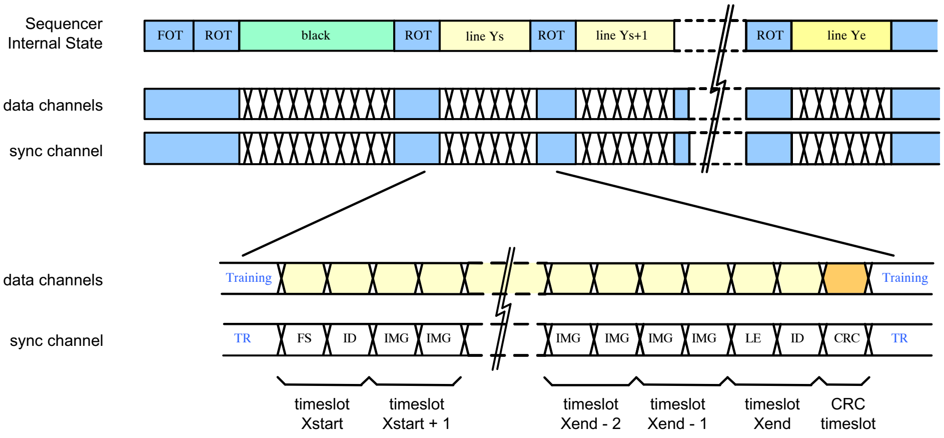


Figure 30. Time Line for Single Window Readout (at the start of a frame)

Figure 31 shows the detail of the readout of a number of lines for readout of two overlapping windows.

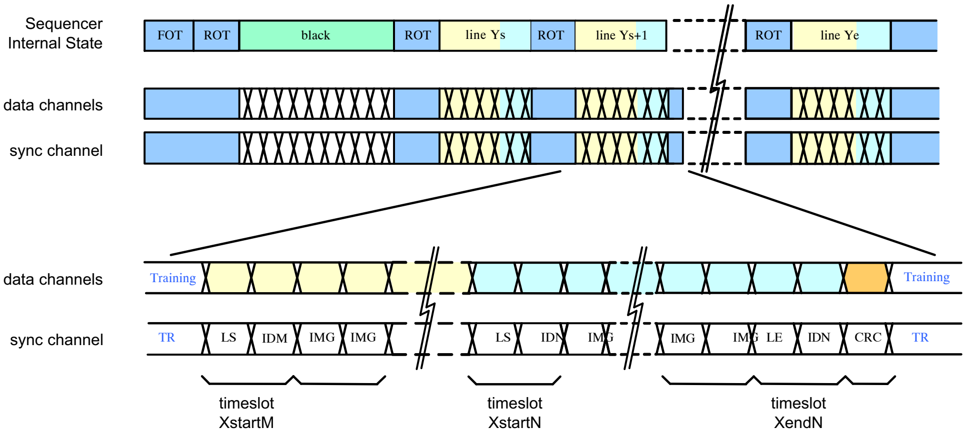


Figure 31. Time Line Showing the Readout of Two Overlapping Windows

Frame Synchronization in 10−bit Mode

Table 30 shows the structure of the frame synchronization code. Note that the table shows the default data word (configurable) for 10-bit mode. If more than one window is active at the same time, the sync channel transmits the frame synchronization codes of the window with highest index only.

Table 29. FRAME SYNCHRONIZATION CODE DETAILS FOR 10-BIT MODE

Sync Word Bit Position	Register Address	Default Value	Description
9:7	N/A	0x5	Frame start indication
9:7	N/A	0x6	Frame end indication
9:7	N/A	0x1	Line start indication
9:7	N/A	0x2	Line end indication
6:0	131[6:0]	0x2A	These bits indicate that the received sync word is a frame synchronization code. The value is programmable by a register setting

- Window Identification

Frame synchronization codes are always followed by a 3-bit window identification (bits 2:0). This is an integer number, ranging from 0 to 7, indicating the active window. If more than one window is active for the current cycle, the highest window ID is transmitted.

- Data Classification Codes

For the remaining cycles, the sync channel indicates the type of data sent through the data links: black pixel data (BL), image data (IMG), or training pattern (TR). These codes are programmable by a register setting. The default values are listed in Table 31.

Table 30. SYNCHRONIZATION CHANNEL DEFAULT IDENTIFICATION CODE VALUES FOR 10-BIT MODE

Sync Word Bit Position	Register Address	Default Value	Description
9:0	132 [9:0]	0x015	Black pixel data (BL). This data is not part of the image. The black pixel data is used internally to correct channel offsets.
9:0	133 [9:0]	0x035	Valid pixel data (IMG). The data on the data output channels is valid pixel data (part of the image).
9:0	134 [9:0]	0x059	CRC value. The data on the data output channels is the CRC code of the finished image data line.
9:0	135 [9:0]	0x3A6	Training pattern (TR). The sync channel sends out the training pattern which can be programmed by a register setting.

Frame Synchronization in 8-bit Mode

The frame synchronization words are configured using the same registers as in 10-bit mode. The two least significant bits of these configuration registers are ignored and not sent out. Table 32 shows the structure of the frame synchronization code, together with the default value, as specified in SPI registers. The same restriction for overlapping windows applies in 8-bit mode.

Table 31. FRAME SYNCHRONIZATION CODE DETAILS FOR 8-BIT MODE

Sync Word Bit Position	Register Address	Default Value	Description
7:5	N/A	0x5	Frame start (FS) indication
7:5	N/A	0x6	Frame end (FE) indication
7:5	N/A	0x1	Line start (LS) indication
7:5	N/A	0x2	Line end (LE) indication
4:0	[6:2]	0x0A	These bits indicate that the received sync word is a frame synchronization code. The value is programmable by a register setting.

- Window Identification

Similar to 10-bit operation mode, the frame synchronization codes are followed by a window identification. The window ID is located in bits 4:2 (all other bit positions are ‘0’). The same restriction for overlapping windows applies in 8-bit mode.

- Data Classification Codes

BL, IMG, CRC, and TR codes are defined by the same registers as in 10-bit mode. Bits 9:2 of the respective configuration registers are used as classification code with default values shown in Table 33.

Table 32. SYNCHRONIZATION CHANNEL DEFAULT IDENTIFICATION CODE VALUES FOR 8-BIT MODE

Sync Word Bit Position	Register Address	Default Value	Description
7:0	132 [9:2]	0x05	Black pixel data (BL). This data is not part of the image. The black pixel data is used internally to correct channel offsets.
7:0	133 [9:2]	0x0D	Valid pixel data (IMG). The data on the data output channels is valid pixel data (part of the image).
7:0	134 [9:2]	0x16	CRC value. The data on the data output channels is the CRC code of the finished image data line.
7:0	135 [9:2]	0xE9	Training Pattern (TR). The sync channel sends out the training pattern which can be programmed by a register setting.

Training Patterns on Data Channels

In 10-bit mode, during idle periods, the data channels transmit training patterns, indicated on the sync channel by a TR code. These training patterns are configurable independent of the training code on the sync channel as shown in Table 34.

In 8-bit mode, the training pattern for the data channels is defined by the same register as in 10-bit mode, where the lower two bits are omitted; see Table 35.

Table 33. TRAINING CODE ON SYNC CHANNEL IN 10-BIT MODE

Sync Word Bit Position	Register Address	Default Value	Description
[9:0]	130 [9:0]	0x3A6	Data channel training pattern. The data output channels send out the training pattern, which can be programmed by a register setting. The default value of the training pattern is 0x3A6, which is identical to the training pattern indication code on the sync channel.

Table 34. TRAINING PATTERN ON DATA CHANNEL IN 8-BIT MODE

Data Word Bit Position	Register Address	Default Value	Description
[7:0]	130 [9:2]	0xE9	Data Channel Training Pattern (Training pattern).

Cyclic Redundancy Code

At the end of each line, a CRC code is calculated to allow error detection at the receiving end. Each data channel transmits a CRC code to protect the data words sent during the previous cycles. Idle and training patterns are not included in the calculation.

The sync channel is not protected. A special character (CRC indication) is transmitted whenever the data channels send their respective CRC code.

The polynomial in 10-bit operation mode is $x^{10} + x^9 + x^6 + x^3 + x^2 + x + 1$. The CRC encoder is seeded at the start of a new line and updated for every (valid) data word received. The CRC seed is configurable using the crc_seed register. When ‘0’, the CRC is seeded by all-‘0’; when ‘1’ it is seeded with all-‘1’.

In 8-bit mode, the polynomial is $x^8 + x^6 + x^3 + x^2 + 1$. The CRC seed is configured by means of the crc_seed register.

Note The CRC is calculated for every line. This implies that the CRC code can protect lines from multiple windows.

Data Order

To read out the image data through the output channels, the pixel array is organized in kernels. The kernel size is eight pixels in x-direction by one pixel in y-direction. Figure 32 indicates how the kernels are organized. The first kernel (kernel [0, 0]) is located in the bottom left corner. The data order of this image data on the data output channels depends on the subsampling mode.

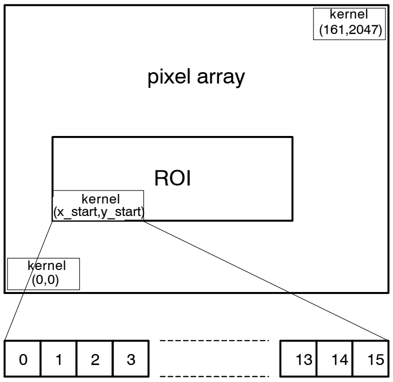


Figure 32. Kernel Organization in Pixel Array

- No Subsampling

The image data is read out in kernels of 16 pixels in x-direction by one pixel in y-direction. One data channel output delivers two pixel values of one kernel sequentially.

Figure 33 shows how a kernel is read out over the eight output channels. For even positioned kernels, the kernels are read out ascending, while for odd positioned kernels the data order is reversed (descending).

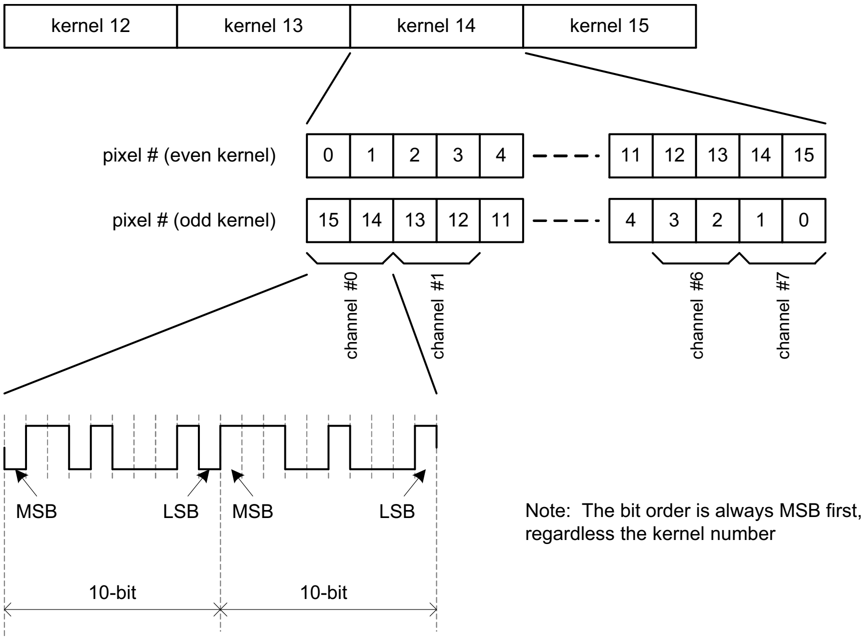


Figure 33. Data Output Order when Subsampling is Disabled

- Subsampling on Monochrome Sensor

To read out the image data with subsampling enabled on a monochrome sensor, two neighboring kernels are combined to a single kernel of 32 pixels in the x-direction and one pixel in the y-direction. Only the pixels at the even pixel positions inside that kernel are read out. Figure 34 shows the data order.

Note that there is no difference in data order for even/odd kernel numbers, as opposed to the ‘no-subsampling’ readout.

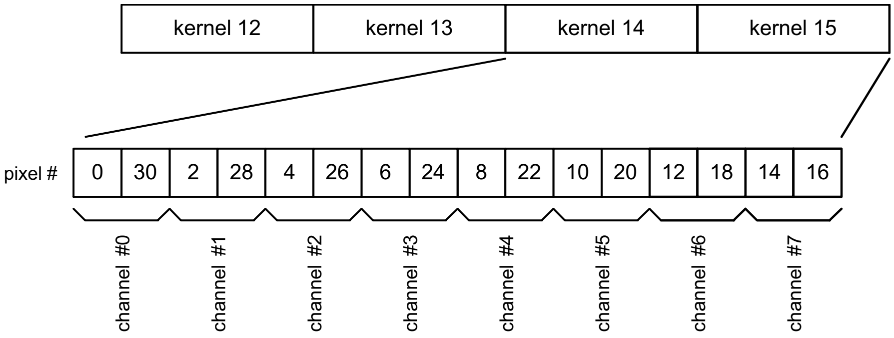


Figure 34. Data Output Order in Subsampling Mode on a Monochrome Sensor

- Subsampling on Color Sensor

To read out the image data with subsampling enabled on a color sensor, two neighboring kernels are combined to a single kernel of 32 pixels in the x-direction and one pixel in the y-direction. Only the pixels 0, 1, 4, 5, 8, 9, 12, and 13 are read out. Figure 35 shows the data order.

Note that there is no difference in data order for even/odd kernel numbers, as opposed to the ‘no-subsampling’ readout.

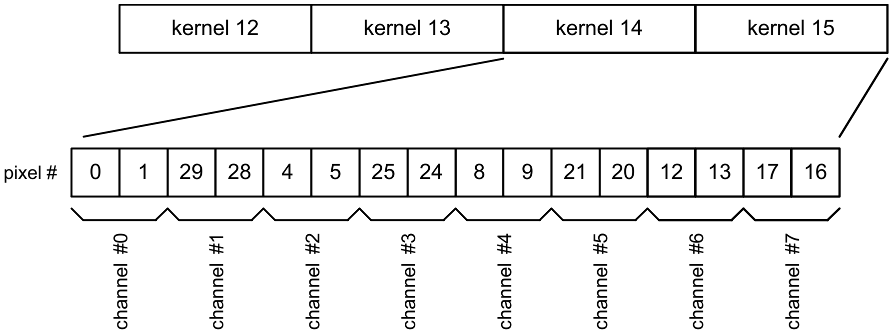


Figure 35. Data Output Order in Subsampling Mode on a Color Sensor

REGISTER MAP

Table 35. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default (Dec)	Description	Type
Chip ID [Block Offset: 0]							
0	0		chip_id	0x5632	22066		RO
		[15:0]	id	0x5632	22066	ON Semiconductor chip ID	
1	1		reserved	0x0000	0		RO
		[3:0]	reserved	0x0000	0	Reserved	
2	2		chip_configuration	0x0000	0		RW
		[1:0]		0x0	0	Configure as per part number: NOIV1SN5000A-QDC: 0x0 NOIV1SE5000A-QDC: 0x1	[0]: color
Reset Generator [Block Offset: 8]							
0	8		soft_reset_pll	0x099	153		RW
		[3:0]	pll_soft_reset	0x9	9	PLL reset 0x9: Soft Reset State Others: Operational	
		[7:4]	pll_lock_soft_reset	0x9	9	PLL Lock Detect Reset 0x9: Soft Reset State Others: Operational	
1	9		soft_reset_cgen	0x09	9		
		[3:0]	cgen_soft_reset	0x9	9	Clock Generator Reset 0x9: Soft Reset State Others: Operational	
2	10		soft_reset_analog	0x0999	2457		
		[3:0]	mux_soft_reset	0x9	9	Column MUX Reset 0x9: Soft Reset State Others: Operational	
		[7:4]	afe_soft_reset	0x9	9	AFE Reset 0x9: Soft Reset State Others: Operational	
		[11:8]	ser_soft_reset	0x9	9	Serializer Reset 0x9: Soft Reset State Others: Operational	
PLL [Block Offset: 16]							
0	16		power_down	0x0004	4		RW
		[0]	pwd_n	0x0	0	PLL Power Down ‘0’ = Power Down, ‘1’ = Operational	
		[1]	enable	0x0	0	PLL Enable ‘0’ = disabled, ‘1’ = enabled	
		[2]	bypass	0x1	1	PLL Bypass ‘0’ = PLL Active, ‘1’ = PLL Bypassed	
1	17		config	0x2113	8467		RW

Table 35. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default (Dec)	Description	Type
		[7:0]	mdiv	0x13	19	M-divider 19: 10-bit LVDS, 15: 8-bit LVDS	
		[12:8]	ndiv	0x1	1	N-divider	
		[14:13]	pdiv	0x1	1	P-divider	
IO [Block Offset: 20]							
0	20		config	0x0000	0		RW
		[0]	clock_in_pwd_n	0x0	0	Power down Clock Input	
		[10:8]	reserved	0x0	0	Reserved	
PLL lock detector [Block Offset: 24]							
0	24		pll_lock	0x0000	0		RO
		[0]	lock	0x0	0	PLL lock indication	
2	26		reserved	0x2280	8832		RW
		[14:0]	reserved	0x2280	8832	Reserved	
3	27		reserved	0x3D2D	15661	Reserved	RW
		[15:0]	reserved	0x3D2D	15661	Reserved	
Clock Generator [Block Offset: 32]							
0	32		config	0x0004	4		RW
		[0]	enable_analog	0x0	0	Enable analog clocks ‘0’ = disabled, ‘1’ = enabled	
		[1]	enable_log	0x0	0	Enable logic clock ‘0’ = disabled, ‘1’ = enabled	
		[2]	select_pll	0x1	1	Input Clock Selection ‘0’ = Select LVDS clock input, ‘1’ = Select PLL clock input	
		[3]	adc_mode	0x0	0	Set operation mode ‘0’ = 10-bit mode, ‘1’ = 8-bit mode	
		[11:8]	reserved	0x0	0	Reserved	
		[14:12]	reserved	0x0	0	Reserved	
General Logic [Block Offset: 34]							
0	34		config	0x0000	0		RW
		[0]	enable	0x0	0	Logic General Enable Configuration ‘0’ = Disable ‘1’ = Enable	
Image Core [Block Offset: 40]							
0	40		image_core_config	0x0000	0		RW
		[0]	imc_pwd_n	0x0	0	Image Core Power Down ‘0’ = powered down, ‘1’ = powered up	

Table 35. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default (Dec)	Description	Type
		[1]	mux_pwd_n	0x0	0	Column Multiplexer Power Down ‘0’ = powered down, ‘1’ = powered up	
		[2]	colbias_enable	0x0	0	Bias Enable ‘0’ = disabled ‘1’ = enabled	
1	41		image_core_config	0xB5A	2906		RW
		[3:0]	dac_ds	0xA	10	Double Slope Reset Level	
		[7:4]	dac_ts	0x5	5	Triple Slope Reset Level	
		[10:8]	dac_antibloom	0x3	3	Anti−Blooming Level	
		[12:11]	dac_vddcasc	0x1	1	VDD Casc Level	
		[13]	testpattern	0x0	0	Testpattern generation in columns	
		[14]	injectlevel	0x0	0	Inject level for testpattern generation	
		[15]	reserved	0x0	0	Reserved	
AFE [Block Offset:48]							
0	48		power_down	0x0000	0		RW
		[0]	pwd_n	0x0	0	Power down for AFE’s (64 columns) ‘0’ = powered down, ‘1’ = powered up	
Bias [Block Offset: 64]							
0	64		power_down	0x0000	0		RW
		[0]	pwd_n	0x0	0	Power down bandgap ‘0’ = powered down, ‘1’ = powered up	
1	65		configuration	0x888B	34955		RW
		[0]	extres	0x1	1	External resistor selection ‘0’ = internal resistor, ‘1’ = external resistor	
		[3:1]	reserved	0x5	5	Reserved	
		[7:4]	imc_colpc_ibias	0x8	8	Column Precharge ibias Configuration	
		[11:8]	imc_colbias_ibias	0x8	8	Column Bias ibias configuration	
		[15:12]	cp_ibias	0x8	8	Charge pump bias	
2	66		afe_bias	0x53C8	21448		RW
		[3:0]	afe_ibias	0x8	8	AFE ibias Configuration	
		[7:4]	afe_adc_iref	0xC	12	ADC iref Configuration	
		[14:8]	afe_pga_iref	0x53	83	PGA iref Configuration	
3	67		mux_bias	0x8888	34952		RW
		[3:0]	mux_25u_stage1	0x8	8	Column Multiplexer Stage 1 Bias Configuration	
		[7:4]	mux_25u_stage2	0x8	8	Column Multiplexer Stage 2 Bias Configuration	
		[11:8]	mux_25u_delay	0x8	8	Column Multiplexer Delay Bias Configuration	

Table 35. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default (Dec)	Description	Type
		[15:8]	mux_25u_vcmbuff	0x8	8	Column Multiplexer Delay Vcm Configuration	
4	68		lvds_bias	0x0088	136		RW
		[3:0]	lvds_ibias	0x8	8	LVDS Ibias	
		[7:4]	lvds_iref	0x8	8	LVDS Iref	
6	70		reserved	0x8888	34952		RW
		[15:0]	reserved	0x8888	34952	Reserved	
Charge Pump [Block Offset: 72]							
0	72		config	0x1200	4608		RW
		[0]	respd_trans_pwd_n	0x0	0	PD Trans Charge Pump Enable ‘0’ = disabled, ‘1’ = enabled	
		[1]	resfd_pwd_n	0x0	0	FD Charge Pump Enable ‘0’ = disabled, ‘1’ = enabled	
		[10:8]	respd_trans_trim	0x2	2	PD Trans Charge Pump Trim	
		[14:12]	resfd_trim	0x1	1	FD Charge Pump Trim	
Reserved [Block Offset: 80]							
0	80		reserved	0x0000	0		RW
		[9:0]	reserved	0x000	0	Reserved	
1	81		config	0x8881	34945		RW
		[15:0]	reserved	0x8881	34945		
Temperature Sensor [Block Offset: 96]							
0	96		sensor enable	0x0000	0		RW
		[0]	reg_tempd_enable	0x0	0	Temperature Diode Enable ‘0’ = disabled ‘1’ = enabled	
1	97		sensor output	0x0000	0		RO
		[7:0]	tempd_reg_temp	0x00	0	Temperature Readout	
Serializer/LVDS [Block Offset: 112]							
0	112		power_down	0x0000	0		RW
		[0]	clock_out_pwd_n	0x0	0	Power down for Clock Output. ‘0’ = powered down, ‘1’ = powered up	
		[1]	sync_pwd_n	0x0	0	Power down for Sync channel ‘0’ = powered down, ‘1’ = powered up	
		[2]	data_pwd_n	0x0	0	Power down for data channels (4 channels) ‘0’ = powered down, ‘1’ = powered up	
Data Block [Block Offset: 128]							
0	128		blackcal	0x4008	16392		RW
		[7:0]	black_offset	0x08	8	Desired black level at output	
		[10:8]	black_samples	0x0	0	Black pixels taken into account for black calibration. Total samples = 2**black_samples	

Table 35. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default (Dec)	Description	Type
		[14:11]	adc_offset	0x8	8	ADC offset = 2**adc_offset. This setting should correspond to the Calibration DAC setting	
		[15]	crc_seed	0x0	0	CRC seed ‘0’ = All 0 ‘1’ = All 1	
1	129		general_configuration	0xC001	49153		RW
		[0]	auto_blackcal_enable	0x1	1	Automatic blackcalibration is enabled when 1, bypassed when 0	
		[9:1]	blackcal_offset	0x00	0	Black Calibration offset used when auto_black_cal_en = ‘0’.	
		[10]	blackcal_offset_dec	0x0	0	blackcal_offset is added when 0, subtracted when 1	
		[11]	compress_bypass	0x0	0	Bypass compression of 11-bit ADC data to 10-bit output data when 1	
		[12]	bypass	0x0	0	Bypass datablock (test only) when ‘1’. Use default value for normal operation.	
		[13]	8bit_mode	0x0	0	Shifts window ID indications by 4 cycles. ‘0’ = 10-bit mode, ‘1’ = 8-bit mode	
2	130		trainingpattern	0x03A6	934		RW
		[9:0]	trainingpattern	0x3A6	934	Training pattern sent on data channels during idle mode. This data is used to perform word alignment on the LVDS data channels.	
		[10]	reserved	0x0	0	Reserved	
3	131		sync_code0	0x002A	42		RW
		[6:0]	frame_sync	0x02A	42	Frame sync LSBs. Note: The tenth bit indicates frame/line sync code, ninth bit indicates start, eighth bit indicates end.	
4	132		sync_code1	0x0015	21		RW
		[9:0]	bl	0x015	21	Black Pixel Identification Sync Code	
5	133		sync_code2	0x0035	53		RW
		[9:0]	img	0x035	53	Valid Pixel Identification Sync Code	
6	134		sync_code3	0x0059	89		RW
		[9:0]	crc	0x059	89	CRC Value Identification Sync Code	
7	135		sync_code4	0x03A6	934		RW
		[9:0]	tr	0x3A6	934	Training Value Identification Sync Code	
8	136		blackcal_error0	0x0000	0		RO

Table 35. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default (Dec)	Description	Type
		[15:0]	blackcal_error[15:0]	0x0000	0	Black Calibration Error. This flag is set when not enough black samples are available. Black Calibration shall not be valid. Channels 0-16 (channels 0–15 for VITA 5000)	
9	137		blackcal_error1	0x0000	0		RO
		[15:0]	blackcal_error[31:16]	0x0000	0	Black Calibration Error. This flag is set when not enough black samples are available. Black Calibration shall not be valid. Channels 16-31 (N/A for VITA 5000)	
10	138		blackcal_error2	0x0000	0		RO
		[15:0]	blackcal_error[47:32]	0x0000	0	Black Calibration Error. This flag is set when not enough black samples are available. Black Calibration shall not be valid. Channels 32-47 (N/A for VITA 5000)	
11	139		blackcal_error3	0x0000	0		RO
		[15:0]	blackcal_error[63:48]	0x0000	0	Black Calibration Error. This flag is set when not enough black samples are available. Black Calibration shall not be valid. Channels 48-63 (N/A for VITA 5000)	
12	140		reserved	0x0000	0		RW
		[15:0]	reserved	0x0000	0	Reserved	
13	141		reserved	0xFFFF	65535		RW
		[15:0]	reserved	0xFFFF	65535	Reserved	
Datablock - Test							
16	144		test_configuration	0x0000	0		RW
		[0]	testpattern_en	0x0	0	Insert synthesized testpattern when ‘1’	
		[1]	inc_testpattern	0x0	0	Incrementing testpattern when ‘1’, constant testpattern when ‘0’	
		[2]	prbs_en	0x0	0	Insert PRBS when ‘1’	
		[3]	frame_testpattern	0x0	0	Frame test patterns when ‘1’, unframed testpatterns when ‘0’	
		[4]	test_adc_select	0x0	0	Configures which ADC of selected channels is selected to output ADC data through adc_dout pins	
17	145		reserved	0x0000	0		RW
		[15:0]	reserved		0	Reserved	
18	146		test_configuration0	0x0100	256		RW
		[7:0]	testpattern0_lsb	0x00	0	Testpattern used on datapath #0 when testpattern_en = ‘1’. Note: Most significant bits are configured in register 150.	

Table 35. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default (Dec)	Description	Type
		[15:8]	testpattern1_lsb	0x01	1	Testpattern used on datapath #1 when testpattern_en = ‘1’. Note: Most significant bits are configured in register 150.	
19	147		test_configuration1	0x0302	770		RW
		[7:0]	testpattern2_lsb	0x02	2	Testpattern used on datapath #2 when testpattern_en = ‘1’. Note: Most significant bits are configured in register 150.	
		[15:8]	testpattern3_lsb	0x03	3	Testpattern used on datapath #3 when testpattern_en = ‘1’. Note: Most significant bits are configured in register 150.	
20	148		test_configuration2	0x0504	1284		RW
		[7:0]	testpattern4_lsb	0x04	4	Testpattern used on datapath #4 when testpattern_en = ‘1’. Note: Most significant bits are configured in register 150.	
		[15:8]	testpattern5_lsb	0x05	5	Testpattern used on datapath #5 when testpattern_en = ‘1’. Note: Most significant bits are configured in register 150.	
21	149		test_configuration3	0x0706	1798		RW
		[7:0]	testpattern6_lsb	0x06	6	Testpattern used on datapath #6 when testpattern_en = ‘1’. Note: Most significant bits are configured in register 150.	
		[15:8]	testpattern7_lsb	0x07	7	Testpattern used on datapath #7 when testpattern_en = ‘1’. Note: Most significant bits are configured in register 150.	
22	150		test_configuration16	0x0000	0		RW
		[1:0]	testpattern0_msb	0x0	0	Testpattern used when testpattern_en = ‘1’	
		[3:2]	testpattern1_msb	0x0	0	Testpattern used when testpattern_en = ‘1’	
		[5:4]	testpattern2_msb	0x0	0	Testpattern used when testpattern_en = ‘1’	
		[7:6]	testpattern3_msb	0x0	0	Testpattern used when testpattern_en = ‘1’	
		[9:8]	testpattern4_msb	0x0	0	Testpattern used when testpattern_en = ‘1’	
		[11:10]	testpattern5_msb	0x0	0	Testpattern used when testpattern_en = ‘1’	
		[13:12]	testpattern6_msb	0x0	0	Testpattern used when testpattern_en = ‘1’	
		[15:14]	testpattern7_msb	0x0	0	Testpattern used when testpattern_en = ‘1’	
26	154		reserved	0x0000	0		RW
		[15:0]	reserved	0x0000	0	Reserved	
27	155		reserved	0x0000	0		RW

Table 35. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default (Dec)	Description	Type
		[15:0]	reserved	0x0000	0	Reserved	
AEC[Block Offset: 160]							
0	160		configuration	0x0010	16		RW
		[0]	enable	0x0	0	AEC enable	
		[1]	restart_filter	0x0	0	Restart AEC filter	
		[2]	freeze	0x0	0	Freeze AEC filter and enforcer gains	
		[3]	pixel_valid	0x0	0	Use every pixel from channel when 0, every 4th pixel when 1	
		[4]	amp_pri	0x1	1	Stage 1 amplifier gets higher priority than Stage 2 gain distribution if 1. vice versa if 0	
1	161		intensity	0x60B8	24760		RW
		[9:0]	desired_intensity	0xB8	184	Target average intensity	
		[13:10]	clipping_threshold_avg	0x018	24	Clipping threshold for average inc factor 3.3 unsigned	
2	162		red_scale_factor	0x0080	128		RW
		[9:0]	red_scale_factor	0x80	128	Red scale factor for white balancing 3.7 unsigned	
3	163		green1_scale_factor	0x0080	128		RW
		[9:0]	green1_scale_factor	0x80	128	Green1 scale factor for white balancing 3.7 unsigned	
4	164		green2_scale_factor	0x0080	128		RW
		[9:0]	green2_scale_factor	0x80	128	Green2 scale factor for white balancing 3.7 unsigned	
5	165		blue_scale_factor	0x0080	128		RW
		[9:0]	blue_scale_factor	0x80	128	Blue scale factor for white balancing 3.7 unsigned	
6	166		exposure	0x03FF	1023		RW
		[15:0]	fixed_exposure	0x03FF	1023	Fixed Exposure Time	
7	167		gain	0x0800	2048		RW
		[1:0]	gain_stage1_select	0x0	0	Fixed Column Amplifier gain	
		[3:2]	gain_stage2_select	0x0	0	Fixed AFE PGA Gain	
		[15:4]	fixed_digital_gain	0x080	128	Fixed digital gain 5.7 unsigned	
8	168		min_exposure	0x0001	1		RW
		[15:0]	min_exposure	0x0001	1	Minimum exposure time	
9	169		min_gain	0x0800	2048		RW
		[1:0]	min_gain_stage1	0x0	0	Minimum gain stage 1	
		[3:2]	min_gain_stage2	0x0	0	Minimum gain stage 2	
		[15:4]	min_digital_gain	0x080	128	Minimum digital gain 5.7 unsigned	
10	170		max_exposure	0x03FF	1023		RW
		[15:0]	max_exposure	0x03FF	1023	Maximum exposure time	

Table 35. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default (Dec)	Description	Type
11	171		max_gain	0x100D	4109		RW
		[1:0]	max_gain_stage1	0x1	1	Maximum gain stage 1	
		[3:2]	max_gain_stage2	0x3	3	Maximum gain stage 2	
		[15:4]	max_digital_gain	0x100	256	Maximum digital gain 5.7 unsigned	
12	172		hysteresis	0x00083	131		RW
		[7:0]	digital_hysteresis	0x083	131	Digital Hysteresis 1.7 unsigned	
		[13:8]	dim_threshold	0x00	0	Dimming Threshold	
		[15:14]	dim_factor	0x0	0	Dimming Factor	
13	173		lock_gain	0x2824	10276		RW
		[7:0]	reserved	0x024	36	Reserved	
		[15:8]	reserved	0x028	40	Reserved	
14	174		loop_gain	0x2A96	10902		RW
		[15:0]	reserved	0x2A96	10902	Reserved	
15	175		reserved	0x0080	128		RW
		[9:0]	reserved	0x080	128	Reserved	
16	176		reserved	0x0100	256		RW
		[9:0]	reserved	0x100	256	Reserved	
17	177		reserved	0x0100	256		RW
		[9:0]	reserved	0x100	256	Reserved	
18	178		reserved	0x0080	128		RW
		[9:0]	reserved	0x080	128	Reserved	
19	179		reserved	0x00AA	170		RW
		[9:0]	reserved	0x0AA	170	Reserved	
20	180		reserved	0x0100	256		RW
		[9:0]	reserved	0x100	256	Reserved	
21	181		reserved	0x0155	341		RW
		[9:0]	reserved	0x155	341	Reserved	
24	184		total_pixels0	0x0000	0		RO
		[15:0]	total_pixels[15:0]	0x0000	0	Total number of pixels sampled for Average, LSB	
25	185		total_pixels1	0x0000	0		RO
		[2:0]	total_pixels[18:16]	0x0	0	Total number of pixels sampled for Average, MSB	
26	186		average_status	0x0000	0		RO
		[9:0]	average	0x000	0	AEC Average Status	
		[12]	locked	0x0	0	AEC Filter Lock Status	
27	187		exposure_status	0x0000	0		RO
		[15:0]	exposure	0x0000	0	AEC Exposure Status	
28	188		gain_status	0x00	0		RO
		[1:0]	gain_stage1	0x0	0	Gain Stage 1 Status	

Table 35. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default (Dec)	Description	Type
		[3:2]	gain_stage2	0x0	0	Gain Stage 2 Status	
		[15:4]	digital_gain	0x000	0	AEC Digital Gain Status 5.7 unsigned	
29	189		reserved	0x0000	0		RO
		[12:0]	reserved	0x000	0	Reserved	
Sequencer [Block Offset: 192]							
0	192		general_configuration	0x00	0		RW
		[0]	enable	0x0	0	Enable sequencer ‘0’ = Idle, ‘1’ = enabled	
		[1]	rolling_shutter_enable	0x0	0	Operation Selection ‘0’ = global shutter, ‘1’ = rolling shutter	
		[2]	zero_rot_enable	0x0	0	Zero ROT mode Selection ‘0’ = Normal ROT, ‘1’ = Zero ROT	
		[3]	x_lag	0x0	0	x–lag in Zero ROT mode ‘0’ = No lag, ‘1’ = Lag	
		[4]	triggered_mode	0x0	0	Triggered Mode Selection (Snapshot Shutter only) ‘0’ = Normal Mode, ‘1’ = Triggered Mode	
		[5]	slave_mode	0x0	0	Master/slave selection (global shutter only) ‘0’ = master, ‘1’ = slave	
		[6]	nzrot_xsm_delay_enable	0x0	0	Insert delay between end of ROT and start of readout in normal ROT readout mode if ‘1’. ROT delay is defined by register xsm_delay	
		[7]	subsampling	0x0	0	Subsampling mode selection ‘0’ = no subsampling, ‘1’ = subsampling	
		[8]	binning	0x0	0	Binning mode selection ‘0’ = no binning, ‘1’ = binning	
		[10]	roi_aec_enable	0x0	0	Enable windowing for AEC statistics. ‘0’ = Subsample all windows ‘1’ = Subsample configured window	
		[13:11]	monitor_select	0x0	0	Control of the monitor pins	
		[14]	pls_mode	0x0	0	Test mode for PLS measurements	
1	193		delay_configuration	0x0000	0		RW
		[7:0]	rs_x_length	0x00	0	X-Readout duration in rolling shutter mode (extends lines with dummy pixels).	

Table 35. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default (Dec)	Description	Type
		[15:8]	xsm_delay	0x00	0	Delay between ROT start and X-readout (Zero ROT mode) Delay between ROT end and X–readout (Normal ROT mode with nzrot_xsm_delay_enable='1')	
2	194		integration_control	0x0004	4		RW
		[0]	dual_slope_enable	0x0	0	Enable Dual Slope (Snapshot mode only)	
		[1]	triple_slope_enable	0x0	0	Enable Triple Slope (Snapshot mode only)	
		[2]	fr_mode	0x1	1	Representation of fr_length. '0': reset length '1': frame length	
		[9:3]	reserved	0x00	0	Reserved	
3	195		roi_active0	0x0001	1		RW
		[7:0]	roi_active[7:0]	0x01	1	Active ROI's selection	
4	196		reserved	0x0000	0		RW
		[15:0]	reserved	0x0000	0	Reserved	
5	197		black_lines	0x0102	258		RW
		[7:0]	black_lines	0x02	2	Number of black lines; minimum is 1 Range 1 – 255	
		[8]	gate_first_line	0x1	1	Blank out first line '0': No blank-out '1': Blank-out	
6	198		dummy_lines	0x0000	0		RW
		[11:0]	dummy_lines	0x000	0	Number of Dummy Lines (Rolling shutter only) Range 0 – 2047	
7	199		mult_timer	0x0001	1		RW
		[15:0]	mult_timer	0x0001	1	Mult timer (Snapshot Shutter only) Defines granularity (unit = 1/System Clock) of exposure and reset_length	
8	200		fr_length	0x0000	0		RW
		[15:0]	fr_length	0x0000	0	Frame/reset length (Snapshot Shutter only) Reset length when fr_mode = '0', Frame length when fr_mode = '1' Granularity defined by mult_timer	
9	201		exposure	0x0000	0		RW
		[15:0]	exposure	0x0000	0	Exposure Time Rolling shutter: granularity lines Global shutter: granularity defined by mult_timer	
10	202		exposure	0x0000	0		RW
		[15:0]	exposure_ds	0x0000	0	Exposure Time (Dual slope) Rolling shutter: N/A Global shutter: granularity defined by mult_timer	

Table 35. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default (Dec)	Description	Type
11	203		exposure	0x0000	0		RW
		[15:0]	exposure_ts	0x0000	0	Exposure Time (Triple slope) Rolling shutter: N/A Global shutter: granularity defined by mult_timer	
12	204		gain_configuration	0x01E2	482		RW
		[4:0]	gain_stage1	0x02	2	Gain stage 1	
		[12:5]	gain_stage2	0xF	15	Gain stage 2	
		[13]	gain_lat_comp	0x0	0	Postpone gain update by 1 frame when ‘1’ to compensate for exposure time updates latency. Gain is applied at start of next frame if ‘0’	
13	205		digital_gain_configuration	0x0080	128		RW
		[11:0]	db_gain	0x080	128	Digital gain	
14	206		sync_configuration	0x033F	831		RW
		[0]	sync_rs_x_length	0x1	1	Update of rs_x_length are not synchronized at start of frame when ‘0’	
		[1]	sync_black_lines	0x1	1	Update of black_lines are not synchronized at start of frame when ‘0’	
		[2]	sync_dummy_lines	0x1	1	Update of dummy_lines are not synchronized at start of frame when ‘0’	
		[3]	sync_exposure	0x1	1	Update of exposure will not be synchronized at start of frame when ‘0’	
		[4]	sync_gain	0x1	1	Update of gain settings (gain_sw, afe_gain) will not be synchronized at start of frame when ‘0’	
		[5]	sync_roi	0x1	1	Update of roi updates (active_roi) will not be synchronized at start of frame when ‘0’	
		[8]	blank_roi_switch	0x1	1	Blank first frame after ROI switching	
		[9]	blank_subsampling_ss	0x1	1	Blank first frame after subsampling/binning mode switching in snapshot shutter mode (always blanked out in rolling shutter mode)	
		[10]	exposure_sync_mode	0x0	0	When ‘0’, exposure configurations are synchronized at the start of FOT. When ‘1’, exposure configurations sync is disabled (continuously syncing). This mode is only relevant for Triggered global master mode, where the exposure configurations are sync’ed at the start of exposure rather than the start of FOT. For all other modes it should be set to ‘0’. Note: Sync is still postponed if sync_exposure=‘0’.	

Table 35. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default (Dec)	Description	Type
16	208		mult_timer_status	0x0000	0		RO
		[15:0]	mult_timer	0x0000	0	Mult Timer Status (Master Snapshot Shutter only)	
17	209		reset_length_status	0x0000	0		RO
		[15:0]	reset_length	0x0000	0	Current Reset Length (not in Slave mode)	
18	210		exposure_status	0x0000	0		RO
		[15:0]	exposure	0x0000	0	Current Exposure Time (not in Slave mode)	
19	211		exposure_ds_status	0x0000	0		RO
		[15:0]	exposure_ds	0x0000	0	Current Exposure Time (not in Slave mode)	
20	212		exposure_ts_status	0x0000	0		RO
		[15:0]	exposure_ts	0x0000	0	Current Exposure Time (not in Slave mode)	
21	213		gain_status	0x0000	0		RO
		[4:0]	gain_stage1	0x00	0	Current Stage 1 Gain	
		[12:5]	gain_stage2	0x00	0	Current Stage 2 Gain	
22	214		digital_gain_status	0x0000	0		RO
		[11:0]	db_gain	0x000	0	Current Digital Gain	
		[12]	dual_slope	0x0	0	Dual Slope Enabled	
		[13]	triple_slope	0x0	0	Triple Slope Enabled	
24	216		reserved	0x7F00	32512		RW
		[14:0]	reserved	0x7F00	32512	Reserved	
25	217		reserved	0x261E	9758		RW
		[14:0]	reserved	0x261E	9758	Reserved	
26	218		reserved	0x160B	5643		RW
		[14:0]	reserved	0x160B	5643	Reserved	
27	219		reserved	0x3E2E	15918		RW
		[14:0]	reserved	0x3E2E	15918	Reserved	
28	220		reserved	0x6368	25448		RW
		[14:0]	reserved	0x6368	25448	Reserved	
29	221		reserved	0x0008	8		RW
		[6:0]	reserved	0x08	8	Reserved	
32	224		reserved	0x3E01	15873		RW
		[3:0]	globres_dummy_rows	0x1	1	Number of dummy lines to be inserted when exposure ends in Snapshot Shutter Mode. Not used during Rolling Shutter mode.	
		[7:4]	globres_row_id	0x0	0	Line ID on during which reset is deasserted in Snapshot Shutter mode. Not used during Rolling Shutter mode.	
		[13:8]	reserved	0x3E	62	Reserved	
33	225		reserved	0x5EF1	24305		RW

Table 35. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default (Dec)	Description	Type
		[15:0]	reserved	0x5EF1	24305	Reserved	
34	226		reserved	0x6000	24576		RW
		[15:0]	reserved	0x6000	24576	Reserved	
35	227		reserved	0x0000	0		RW
		[15:0]	reserved	0x0000	0	Reserved	
36	228		reserved	0xFFFF	65535		RW
		[15:0]	reserved	0xFFFF	65535	Reserved	
58	250		reserved	0x0422	1058		RW
		[4:0]	reserved	0x02	2	Reserved	
		[9:5]	reserved	0x01	1	Reserved	
		[14:10]	reserved	0x01	1	Reserved	
59	251		reserved	0x30F	783		RW
		[7:0]	reserved	0xF	15	Reserved	
		[15:8]	reserved	0x3	3	Reserved	
60	252		reserved	0x0601	1537		RW
		[7:0]	reserved	0x1	1	Reserved	
		[15:8]	reserved	0x6	6	Reserved	
61	253		roi_aec_configuration0	0x0000	0		RW
		[7:0]	x_start	0x00	0	AEC ROI X Start Configuration (used for AEC statistics when roi_aec_enable=‘1’)	
		[15:8]	x_end	0x0	0	AEC ROI X End Configuration (used for AEC statistics when roi_aec_enable=‘1’)	
62	254		roi_aec_configuration1	0x0000	0		RW
		[12:0]	y_start	0x000	0	AEC ROI Y Start Configuration (used for AEC statistics when roi_aec_enable=‘1’)	
63	255		roi_aec_configuration2	0x0000	0		RW
		[12:0]	y_end	0x0	0	AEC ROI Y End Configuration (used for AEC statistics when roi_aec_enable=‘1’)	
Sequencer ROI [Block Offset: 256]							
0	256		roi0_configuration0	0xA100	41216		RW
		[7:0]	x_start	0x00	0	ROI 0 X Start Configuration	
		[15:8]	x_end	0xA1	161	ROI 0 X End Configuration	
1	257		roi0_configuration1	0x0000	0		RW
		[10:0]	y_start	0x000	0	ROI 0 Y Start Configuration	
2	258		roi0_configuration2	0x07FF	2047		RW
		[10:0]	y_end	0x7FF	2047	ROI 0 Y End Configuration	
3	259		roi1_configuration0	0xA100	41216		RW
		[7:0]	x_start	0x00	0	ROI 1 X Start Configuration	
		[15:8]	x_end	0xA1	161	ROI 1 X End Configuration	
4	260		roi1_configuration1	0x0000	0		RW

Table 35. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default (Dec)	Description	Type
		[10:0]	y_start	0x000	0	ROI 1 Y Start Configuration	
5	261		roi1_configuration2	0x07FF	2047		RW
		[10:0]	y_end	0x7FF	2047	ROI 1 Y End Configuration	
6	262		roi2_configuration0	0xA100	61184		RW
		[7:0]	x_start	0x00	0	ROI 2 X Start Configuration	
		[15:8]	x_end	0xA1	161	ROI 2 X End Configuration	
7	263		roi2_configuration1	0x0000	0		RW
		[10:0]	y_start	0x000	0	ROI 2 Y Start Configuration	
8	264		roi2_configuration2	0x07FF	2047		RW
		[10:0]	y_end	0x7FF	2047	ROI 2 Y End Configuration	
9	265		roi3_configuration0	0xA100	41216		RW
		[7:0]	x_start	0x00	0	ROI 3 X Start Configuration	
		[15:8]	x_end	0xA1	161	ROI 3 X End Configuration	
10	266		roi3_configuration1	0x0000	0		RW
		[10:0]	y_start	0x000	0	ROI 3 Y Start Configuration	
11	267		roi3_configuration2	0x07FF	2047		RW
		[10:0]	y_end	0x7FF	2047	ROI 3 Y End Configuration	
12	268		roi4_configuration0	0xA100	61184		RW
		[7:0]	x_start	0x00	0	ROI 4 X Start Configuration	
		[15:8]	x_end	0xA1	161	ROI 4 X End Configuration	
13	269		roi4_configuration1	0x0000	0		RW
		[10:0]	y_start	0x000	0	ROI 4 Y Start Configuration	
14	270		roi4_configuration2	0x07FF	2047		RW
		[10:0]	y_end	0x7FF	2047	ROI 4 Y End Configuration	
15	271		roi5_configuration0	0xA100	61184		RW
		[7:0]	x_start	0x00	0	ROI 5 X Start Configuration	
		[15:8]	x_end	0xA1	161	ROI 5 X End Configuration	
16	272		roi5_configuration1	0x0000	0		RW
		[10:0]	y_start	0x000	0	ROI 5 Y Start Configuration	
17	273		roi5_configuration2	0x07FF	2047		RW
		[10:0]	y_end	0x7FF	2047	ROI 5 Y End Configuration	
18	274		roi6_configuration0	0xA100	41216		RW
		[7:0]	x_start	0x00	0	ROI 6 X Start Configuration	
		[15:8]	x_end	0xA1	161	ROI 6 X End Configuration	
19	275		roi6_configuration1	0x0000	0		RW
		[10:0]	y_start	0x000	0	ROI 6 Y Start Configuration	
20	276		roi6_configuration2	0x07FF	2047		RW
		[10:0]	y_end	0x7FF	2047	ROI 6 Y End Configuration	
21	277		roi7_configuration0	0xA100	41216		RW
		[7:0]	x_start	0x00	0	ROI 7 X Start Configuration	
		[15:8]	x_end	0xA1	161	ROI 7 X End Configuration	

Table 35. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default (Dec)	Description	Type
22	278		roi7_configuration1	0x0000	0		RW
		[10:0]	y_start	0x000	0	ROI 7 Y Start Configuration	
23	279		roi7_configuration2	0x07FF	2047		RW
		[10:0]	y_end	0x7FF	2047	ROI 7 Y End Configuration	
Reserved [Block Offset: 384]							
0	384		reserved				RW
		[15:0]	reserved			Reserved	
…	…		…				RW
			…			…	
127	511		reserved				RW
		[15:0]	reserved			Reserved	

PACKAGE SPECIFICATIONS

Pin List

The LVDS I/Os comply with the TIA/EIA−644−A standard.

Table 36. PIN LIST

Pack Pin No.	Pin Name	I/O	Direction	Description
1	Mosi	CMOS	Input	SPI Master Out Slave In
2	Miso	CMOS	Output	SPI Master In Slave Out
3	Sclk	CMOS	Input	SPI Input Clock
4	gnd_18	Supply		1.8 V Ground
5	vdd_18	Supply		1.8 V Supply
6	clock_outn	LVDS	Output	LVDS Clock Output (Negative)
7	clock_outp	LVDS	Output	LVDS Clock Output (Positive)
8	doutn0	LVDS	Output	LVDS Data Output Channel #0 (Negative)
9	doutp0	LVDS	Output	LVDS Data Output Channel #1 (Positive)
10	NC	No Connect	No Connect	Not Connected
11	doutn1	LVDS	Output	LVDS Data Output Channel #1 (Negative)
12	doutp1	LVDS	Output	LVDS Data Output Channel #1 (Positive)
13	doutn2	LVDS	Output	LVDS Data Output Channel #2 (Negative)
14	doutp2	LVDS	Output	LVDS Data Output Channel #2 (Positive)
15	doutn3	LVDS	Output	LVDS Data Output Channel #3 (Negative)
16	doutp3	LVDS	Output	LVDS Data Output Channel #3 (Positive)
17	gnd_18	Supply		1.8 V Ground
18	vdd_18	Supply		1.8 V Supply
19	vdd_33	Supply		3.3 V Supply
20	gnd_33	Supply		3.3 V Ground
21	doutn4	LVDS	Output	LVDS Data Output Channel #4 (Negative)
22	doutp4	LVDS	Output	LVDS Data Output Channel #4 (Positive)
23	doutn5	LVDS	Output	LVDS Data Output Channel #5 (Negative)
24	doutp5	LVDS	Output	LVDS Data Output Channel #5 (Positive)
25	doutn6	LVDS	Output	LVDS Data Output Channel #6 (Negative)
26	doutp6	LVDS	Output	LVDS Data Output Channel #6 (Positive)
27	doutn7	LVDS	Output	LVDS Data Output Channel #7 (Negative)
28	doutp7	LVDS	Output	LVDS Data Output Channel #7 (Positive)
29	syncn	LVDS	Output	LVDS Sync Channel Output (Negative)
30	syncp	LVDS	Output	LVDS Sync Channel Output (Positive)
31	vdd_33	Supply		3.3 V Supply
32	gnd_33	Supply		3.3 V Ground
33	gnd_18	Supply		1.8 V Ground
34	vdd_18	Supply		1.8 V Supply
35	lvds_clock_inn	LVDS	Input	LVDS Clock Input (Positive)
36	lvds_clock_inp	LVDS	Input	LVDS Clock Input (Positive)
37	clk_pll	CMOS	Input	Reference Clock Input for PLL
38	vdd_18	Supply		1.8 V Supply

Table 36. PIN LIST

Pack Pin No.	Pin Name	I/O	Direction	Description
39	gnd_18	Supply		1.8 V Ground
40	ibias_master	Analog	I/O	Master Bias Reference
41	vdd_33	Supply		3.3 V Supply
42	gnd_33	Supply		3.3 V Ground
43	vdd_pix_low	Supply		Additional **optional** supply. If not used, tie this node to vdd_pix or ground.
44	NC	No Connect	No Connect	Not Connected
45	NC	No Connect	No Connect	Not Connected
46	vdd_pix	Supply		Pixel Array Supply (3.3 V)
47	gnd_colpc	Supply		Pixel Array Ground (0 V)
48	vdd_pix	Supply		Pixel Array Supply (3.3 V)
49	gnd_colpc	Supply		Pixel Array Ground (0 V)
50	gnd_33	Supply		3.3 V Ground
51	vdd_33	Supply		3.3 V Supply
52	vdd_pix_low	Supply		Additional **optional** supply. If not used, tie this node to vdd_pix or ground.
53	gnd_colpc	Supply		Pixel Array Ground (0 V)
54	vdd_pix	Supply		Pixel Array Supply (3.3 V)
55	gnd_colpc	Supply		Pixel Array Ground (0 V)
56	vdd_pix	Supply		Pixel Array Supply (3.3 V)
57	trigger0	CMOS	Input	Trigger Input #0
58	trigger1	CMOS	Input	Trigger Input #1
59	trigger2	CMOS	Input	Trigger Input #0
60	monitor0	CMOS	Output	Monitor Output #0
61	vdd_pix_low	Supply		Additional **optional** supply. If not used, tie this node to vdd_pix or ground.
62	vdd_33	Supply		3.3 V supply
63	gnd_33	Supply		3.3 V Ground
64	monitor1	CMOS	Output	Monitor Output #1
65	reset_n	CMOS	Input	Sensor Reset (Active Low)
66	ss_n	CMOS	Input	SPI Slave Select.
67	gnd_33	Supply		3.3 V Ground
68	vdd_33	Supply		3.3 V supply

Package Specification

Table 37. MECHANICAL SPECIFICATION FOR VITA 5000 CERAMIC LCC PACKAGE AND BARE DIE

Parameter	Description	Min	Typ	Max	Units
Die (Refer to Figure 37 showing Pin 1 reference as left center)	Die thickness	NA	750	NA	μm
	Die Size		14.7 x 13.9		mm²
	Die center, X offset to the center of package	-50	0	50	μm
	Die center, Y offset to the center of the package	-50	0	50	μm
	Die position, tilt to the Die Attach Plane	-1	0	1	deg
	Die rotation accuracy (referenced to die scribe and lead fingers on package on all four sides)	-1	0	1	deg
	Optical center referenced from the die/package center (X-dir)		–232.28		μm
	Optical center referenced from the die/package center (Y-dir)		1521.2		μm
	Distance from PCB plane to top of the die surface		1.77		mm
	Distance from top of the die surface to top of the glass lid		0.94		mm
Glass Lid Specification	XY size	(-10%)	23.5 x 23.5	(+10%)	mm²
	Thickness	0.5	0.55	0.6	mm
	Spectral response range	400		1000	nm
	Transmission of glass lid (refer to Figure 38)			92	%
Mechanical Shock	JESD22-B104C; Condition G			2000	G
Vibration	JESD22-B103B; Condition 1	20		2000	Hz
Mounting Profile	Reflow profile according to J-STD-020D.1			260	°C
Recommended Socket	Andon Electronics Corporation (www.andonelectronics.com)	620-68-SM-G10-L14-X			

Package Outline Drawing

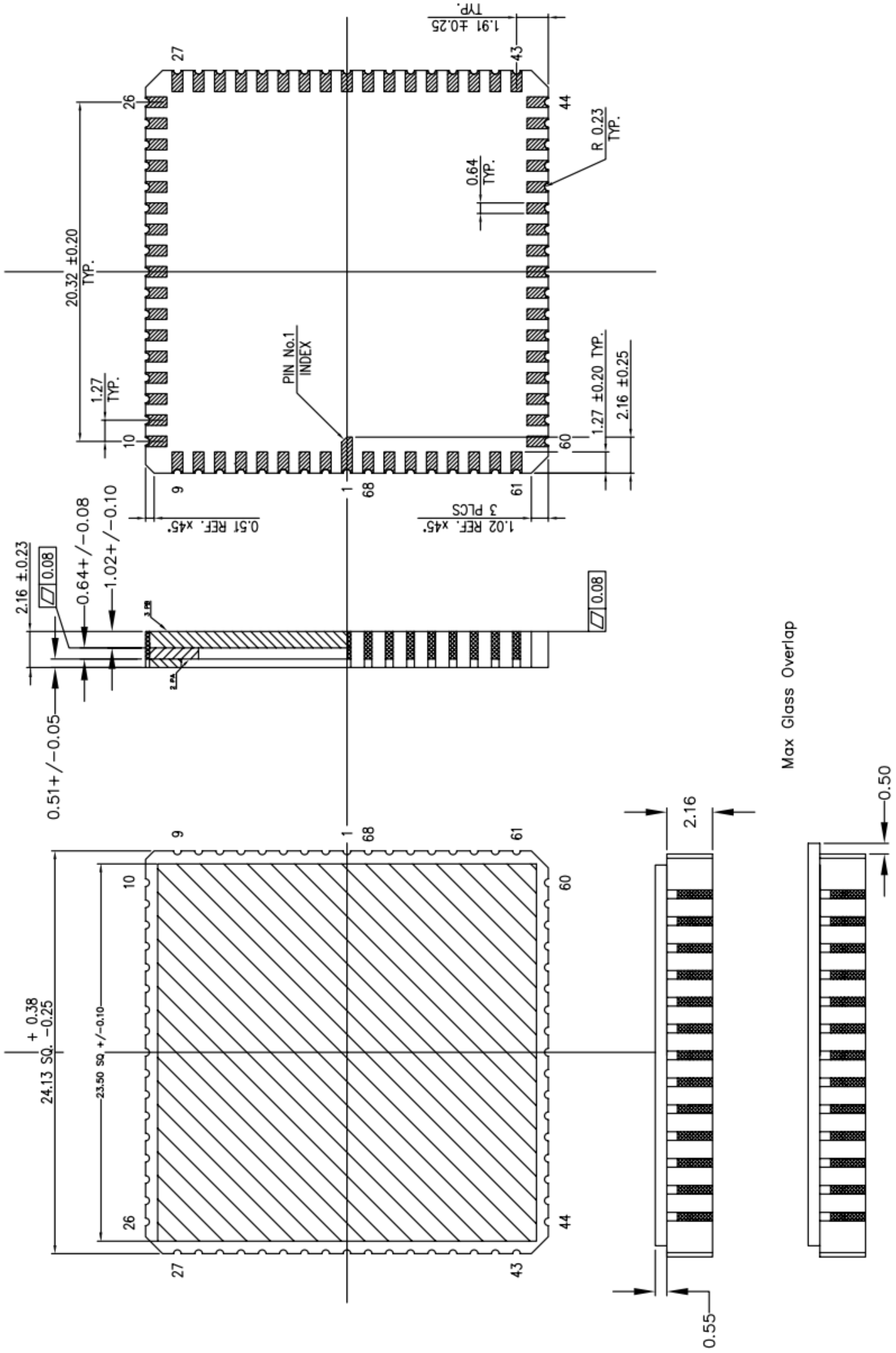


Figure 36. 68−Pin LCC Package (dimensions in mm)

Optical Center Information

The center of the die (CD) is the center of the cavity

The center of the die (CD) is exactly at 50% between the outsides of the two outer seal rings

The center of the cavity is exactly at 50% between the insides of the finger pads.

- Die outer dimensions:
  - B4 is the reference for the Die (0,0) in µm
  - B1 is at (0,13900) µm
  - B2 is at (14700,13900) µm
  - B3 is at (14700,0) µm
- Active Area outer dimensions
  - A1 is the at (880.1, 13403.2) µm
  - A2 is at (13355.3, 13403.2) µm
  - A3 is at (13355.3, 3539.2) µm
  - A4 is at (880.1, 3539.2) µm
- Center of the Active Area
  - AA is at (7117.72, 8471.2) µm
- Center of the Die
  - CD is at (7350, 6950) µm

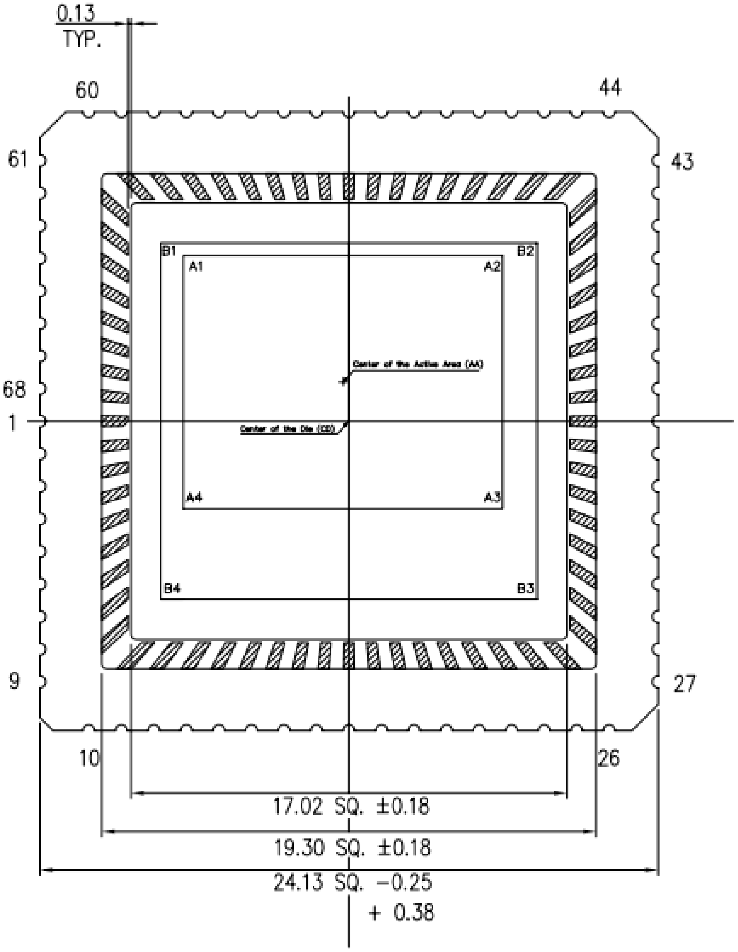


Figure 37. Graphical Representation of the Optical Center

Glass Lid

The VITA 5000 image sensor uses a glass lid without any coatings. Figure 38 shows the transmission characteristics of the glass lid.

As shown in Figure 38, no infrared attenuating color filter glass is used. A filter must be provided in the optical path when color devices are used (source: http://www.pgo-online.com).

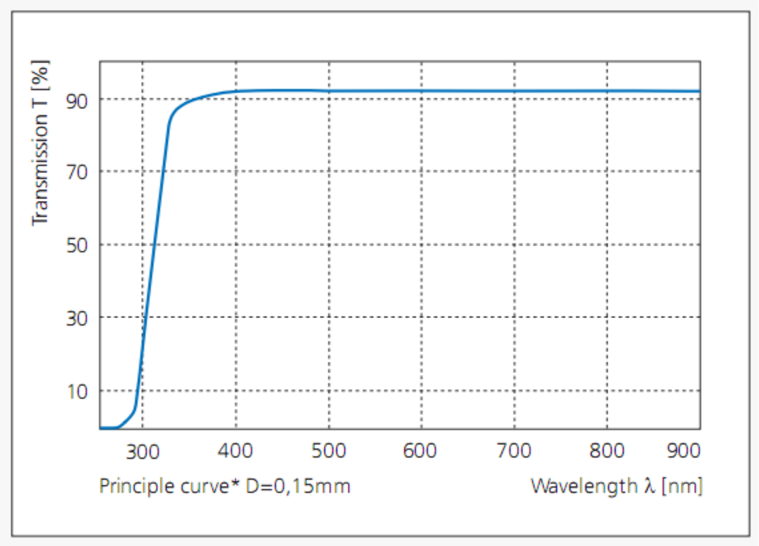


Figure 38. Transmission Characteristics of the Glass Lid

ADDITIONAL REFERENCES AND RESOURCES

Application Notes and other resources can be found linked to the product web page at www.onsemi.com. Additional information on this device may also be available in the Image Sensor Portal, accessible within the MyON section of www.onsemi.com. A signed NDA is required to access the Image Sensor Portal – please see your ON Semiconductor sales representative for more information.

For information on ESD and cover glass care and cleanliness, please download the Application Note *Image Sensor Handling and Best Practices* (AN52561/D) from www.onsemi.com.

For quality and reliability information, please download the *Quality & Reliability Handbook* (HBD851/D) from www.onsemi.com.

For information on Standard terms and Conditions of Sale, please download Terms and Conditions document from www.onsemi.com.

For information on Return Material Authorization procedures, please refer to the RMA Policy Procedure document from www.onsemi.com.

The Product Acceptance Criteria document, which lists criteria to which this device is tested prior to shipment, is available upon request.

SILICON ERRATA

This document describes the errata for the VITA 5000 family. Details include scope of impact, available workaround, and silicon revision applicability. Compare this document to the device’s data sheet for a complete functional description.

Contact your local Sales Representative if you have questions.

Errata Summary

This table defines how the errata applies to the VITA 5000 family.

Items	Part Number	Silicon revision	Fix Status
[1]. Higher Standby current than rated in data sheet	VITA 5000 family	Production Silicon (same as “ES2”)	Silicon fix planned

VITA 5000 Qualification Status

Production Silicon

Higher Standby Current

- PROBLEM DEFINITION

In all states except for ‘idle’ and ‘running’ (including ‘reset’) there can be abnormal high power consumption on vdd_33, up to 300 mW.

- PARAMETERS AFFECTED

Power

- TRIGGER CONDITION(S)

Entering an affected state (reset, low−power standby, standby(1), standby(2)).

- SCOPE OF IMPACT

High power consumption, not influencing performance when grabbing images.

- WORKAROUND

Maintain the device in ‘power−off’, ‘idle’ or ‘running’ modes.

- FIX STATUS

The cause of this problem and its solution have been identified. Silicon fix is planned to correct the deficiency.

- COMPLETION DATE

Production silicon with Stand−by current fix is planned.

Items	Part Number	Silicon revision	Fix Status
[2]. Rolling shutter mode has first line brighter than the remainder rows in uniform illumination	VITA 5000 family	Production Silicon (same as “ES2”)	No silicon fix planned

Rolling Shutter Mode: First row is brighter in uniform illumination

- PROBLEM DEFINITION

The first line(s) are brighter than the remainder rows in uniform illumination due to blooming.

- PARAMETERS AFFECTED

Image artifact: Brighter row(s)

- TRIGGER CONDITION(S)

Artifact observed in rolling shutter mode only.

- SCOPE OF IMPACT

First 1 to 5 rows may show the blooming effect. Refer to the VITA 5000 Acceptance Criteria Specification for production test criteria.

- WORKAROUND

Maximum resolution of actual image is 2592 x 2043.

- FIX STATUS

The cause of this problem has been identified. No silicon fix is planned to correct the deficiency.

- COMPLETION DATE

Not applicable.

ACRONYMS

Acronym	Description
ADC	Analog-to-Digital Converter
AFE	Analog Front End
BL	Black pixel data
CDM	Charged Device Model
CDS	Correlated Double Sampling
CMOS	Complementary Metal Oxide Semiconductor
CRC	Cyclic Redundancy Check
DAC	Digital-to-Analog Converter
DDR	Double Data Rate
DNL	Differential Non-Linearity
DS	Double Sampling
DSNU	Dark Signal Non-Uniformity
EIA	Electronic Industries Alliance
ESD	Electrostatic Discharge
FE	Frame End
FF	Fill Factor
FOT	Frame Overhead Time
FPGA	Field Programmable Gate Array
FPN	Fixed Pattern Noise
FPS	Frame per Second
FS	Frame Start
HBM	Human Body Model
IMG	Image data (regular pixel data)
INL	Integral Non-Linearity

Acronym	Description
IP	Intellectual Property
LE	Line End
LS	Line Start
LSB	least significant bit
LVDS	Low-Voltage Differential Signaling
msb	most significant bit
PGA	Programmable Gain Amplifier
PLS	Parasitic Light Sensitivity
PRBS	Pseudo-Random Binary Sequence
PRNU	Photo Response Non-Uniformity
QE	Quantum Efficiency
RGB	Red-Green-Blue
RMA	Return Material Authorization
rms	Root Mean Square
ROI	Region of Interest
ROT	Row Overhead Time
S/H	Sample and Hold
SNR	Signal-to-Noise Ratio
SPI	Serial Peripheral Interface
TIA	Telecommunications Industry Association
T_J	Junction temperature
TR	Training pattern
% RH	Percent Relative Humidity

GLOSSARY

conversion gain	A constant that converts the number of electrons collected by a pixel into the voltage swing of the pixel. Conversion gain = q/C where q is the charge of an electron (1.602E 19 Coulomb) and C is the capacitance of the photodiode or sense node.
CDS	Correlated double sampling. This is a method for sampling a pixel where the pixel voltage after reset is sampled and subtracted from the voltage after exposure to light.
CFA	Color filter array. The materials deposited on top of pixels that selectively transmit color.
DNL	Differential non-linearity (for ADCs)
DSNU	Dark signal non-uniformity. This parameter characterizes the degree of non-uniformity in dark leakage currents, which can be a major source of fixed pattern noise.
fill-factor	A parameter that characterizes the optically active percentage of a pixel. In theory, it is the ratio of the actual QE of a pixel divided by the QE of a photodiode of equal area. In practice, it is never measured.
INL	Integral nonlinearity (for ADCs)
IR	Infrared. IR light has wavelengths in the approximate range 750 nm to 1 mm.
Lux	Photometric unit of luminance (at 550 nm, 1lux = 1 lumen/m^2 = 1/683 W/m^2)
pixel noise	Variation of pixel signals within a region of interest (ROI). The ROI typically is a rectangular portion of the pixel array and may be limited to a single color plane.
photometric units	Units for light measurement that take into account human physiology.
PLS	Parasitic light sensitivity. Parasitic discharge of sampled information in pixels that have storage nodes.
PRNU	Photo-response non-uniformity. This parameter characterizes the spread in response of pixels, which is a source of FPN under illumination.
QE	Quantum efficiency. This parameter characterizes the effectiveness of a pixel in capturing photons and converting them into electrons. It is photon wavelength and pixel color dependent.
read noise	Noise associated with all circuitry that measures and converts the voltage on a sense node or photodiode into an output signal.
reset	The process by which a pixel photodiode or sense node is cleared of electrons. ”Soft” reset occurs when the reset transistor is operated below the threshold. ”Hard” reset occurs when the reset transistor is operated above threshold.
reset noise	Noise due to variation in the reset level of a pixel. In 3T pixel designs, this noise has a component (in units of volts) proportionality constant depending on how the pixel is reset (such as hard and soft). In 4T pixel designs, reset noise can be removed with CDS.
responsivity	The standard measure of photodiode performance (regardless of whether it is in an imager or not). Units are typically A/W and are dependent on the incident light wavelength. Note that responsivity and sensitivity are used interchangeably in image sensor characterization literature so it is best to check the units.
ROI	Region of interest. The area within a pixel array chosen to characterize noise, signal, crosstalk, and so on. The ROI can be the entire array or a small subsection; it can be confined to a single color plane.
sense node	In 4T pixel designs, a capacitor used to convert charge into voltage. In 3T pixel designs it is the photodiode itself.
sensitivity	A measure of pixel performance that characterizes the rise of the photodiode or sense node signal in Volts upon illumination with light. Units are typically V/(W/m^2)/sec and are dependent on the incident light wavelength. Sensitivity measurements are often taken with 550 nm incident light. At this wavelength, 1 683 lux is equal to 1 W/m^2; the units of sensitivity are quoted in V/lux/sec. Note that responsivity and sensitivity are used interchangeably in image sensor characterization literature so it is best to check the units.
spectral response	The photon wavelength dependence of sensitivity or responsivity.
SNR	Signal-to-noise ratio. This number characterizes the ratio of the fundamental signal to the noise spectrum up to half the Nyquist frequency.
temporal noise	Noise that varies from frame to frame. In a video stream, temporal noise is visible as twinkling pixels.

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